CHANGING WHAT'S POSSIBLE

ENLITENED 2018 Review – TeraPHY for in-package optics

Roy Meade
Ayar Labs

November 16, 2018

TeraPHY for in-package optics

Ayar Labs

Technology Summary

CMOS optical transceivers
co-packaged with processor/switch

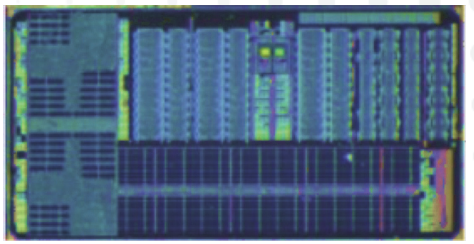
Technology Impact

This project will enable a 2x increase in data center energy efficiency by co-packaging high-bandwidth 1 pJ/b CMOS optical transceivers with switch and processor chips to displace power-hungry electrical links and enable new data center architectures

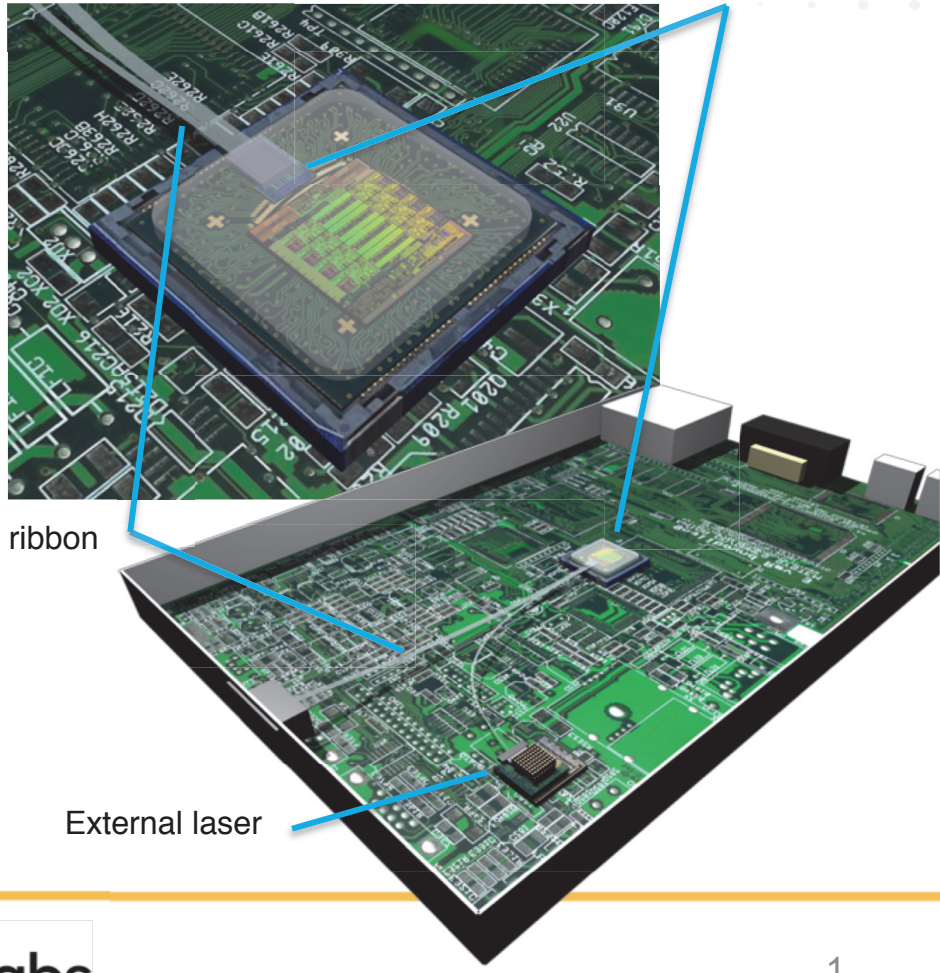
Technical Approach

- 100ºC operation temperature for CMOS optical I/O
- Separate laser with lower temperature requirements
- High volume fiber alignment to CMOS chip
- Standard CMOS manufacturing & assembly techniques

Technology breakthrough:
On-chip optical I/O (top) with dual-core RISC-V processor (left) and memory bank (bottom),
Ref: DARPA POEM,
Sun, C. et al, *Nature* Dec. 2015



Ayar Labs photonic transceiver co-packaged with switch chip



Ayar Labs ENLITENED Team

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CTO and co-founder

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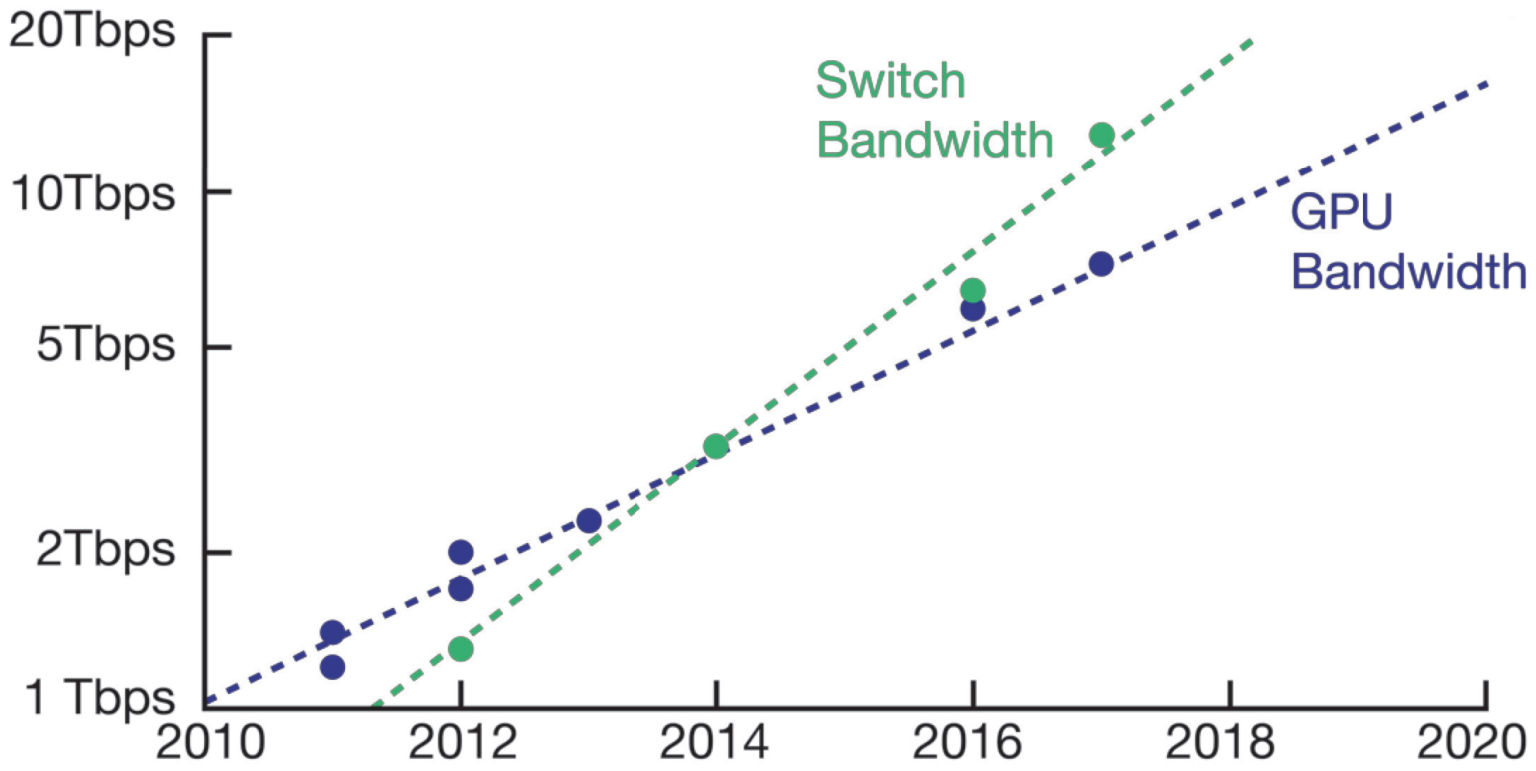
VP of Manufacturing

John Fini, PhD
Principal Engineer

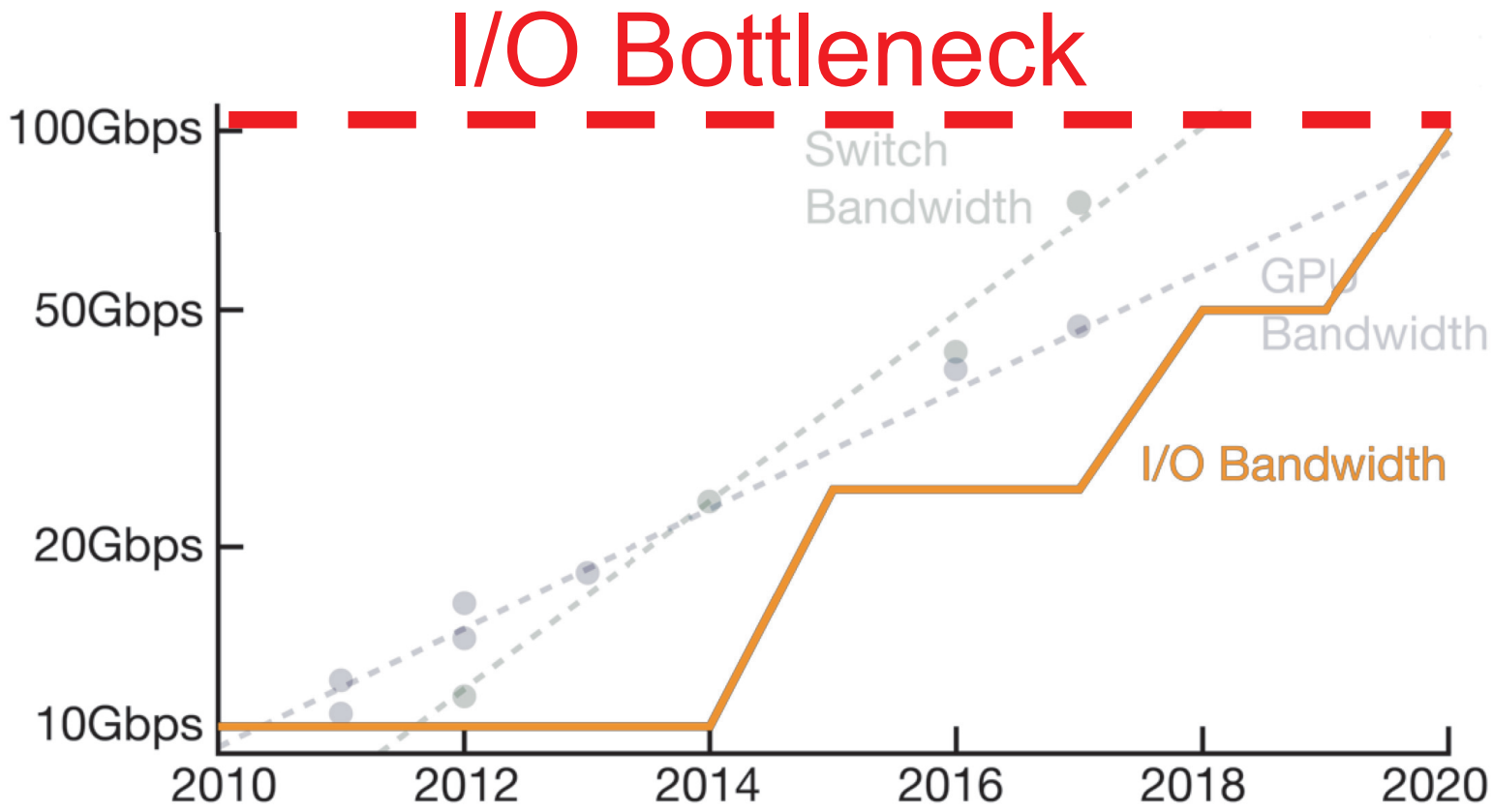
Shahab Ardalan, PhD
Principal Engineer

Chip Capacity Growth



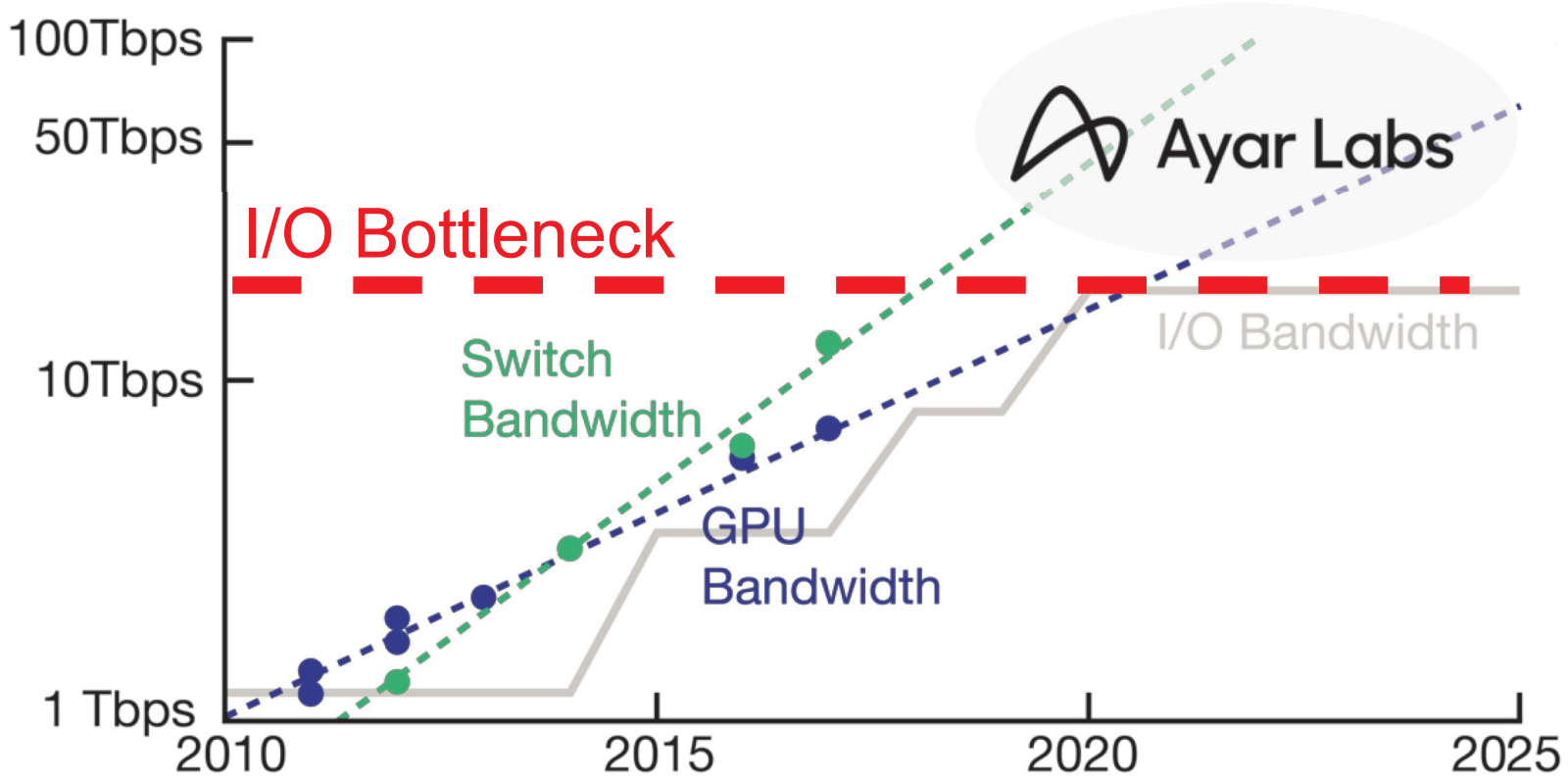
Sources: Product spec sheets. Data available upon request.

The Limits of Copper



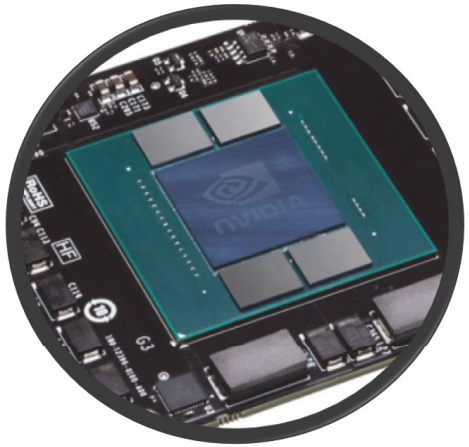
Sources: Wikipedia 10GE, 25GE, Gigabit Ethernet pages

>2020 A New Solution is Needed

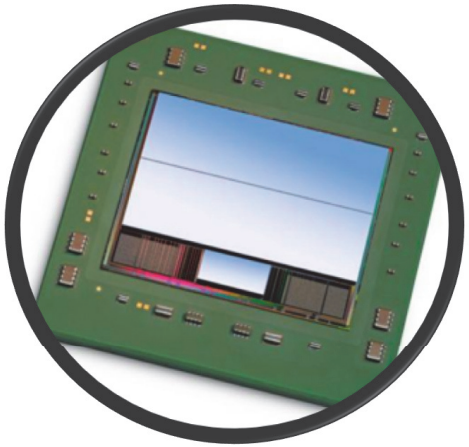


Sources: Product spec sheets. Data available upon request.

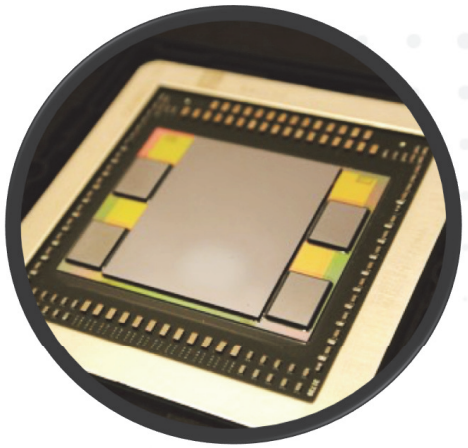
Industry Already Moved to MCMs



nVIDIA Tesla P100

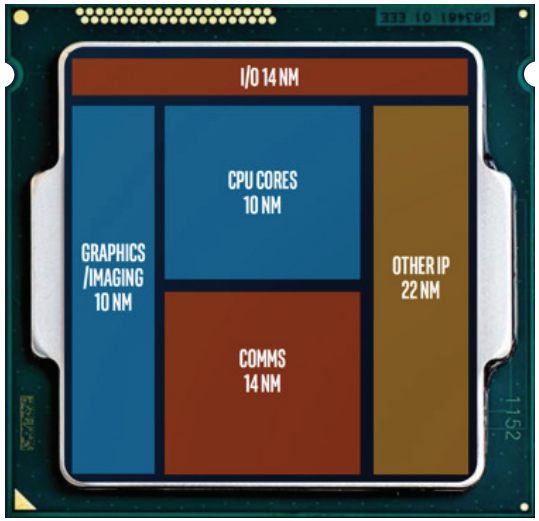


Xilinx Virtex-7 HT



AMD Radeon R9 Fury X

- Mix die function
  - GPU, CPU, memory, I/O, etc.
- Diverse processes & nodes
  - E.g. 16nm,10nm, DRAM, etc.
- Manage yield
- For optics to fit into this ecosystem, must look like electronics!



Outline

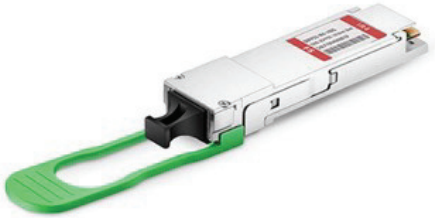
- Constraints of optical I/O in MCMs
- TeraPHY optical I/O
- Fiber-attach for TeraPHY

Constraints of Co-packaged Optics

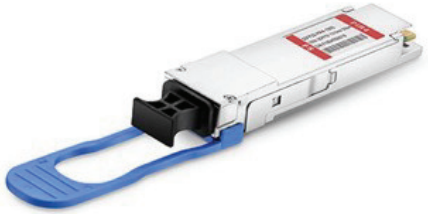
- Bandwidth density
  - Need >100Gbps/mm2 of optical bandwidth density
- Power efficiency
  - <2pJ/bit dissipated in the package (100W at 50Tb/s)
- Thermal environment
  - Up to 400W dissipated and 115ºC in the package
- Co-packaging complexity
  - Need to simplify package!

Co-packaging requires radically new Optics

100G
Pluggables



Next-Gen 400G
Pluggables



Co-packaging requires radically new Optics

100G
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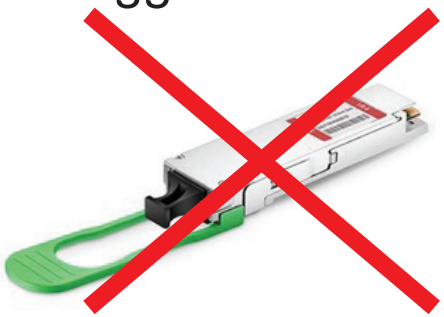

Next-Gen 400G
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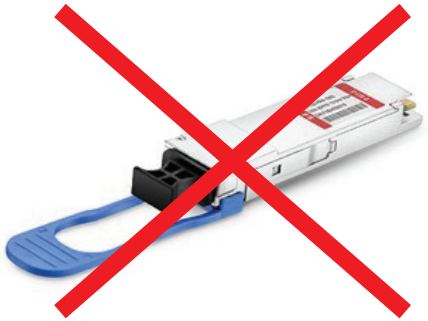
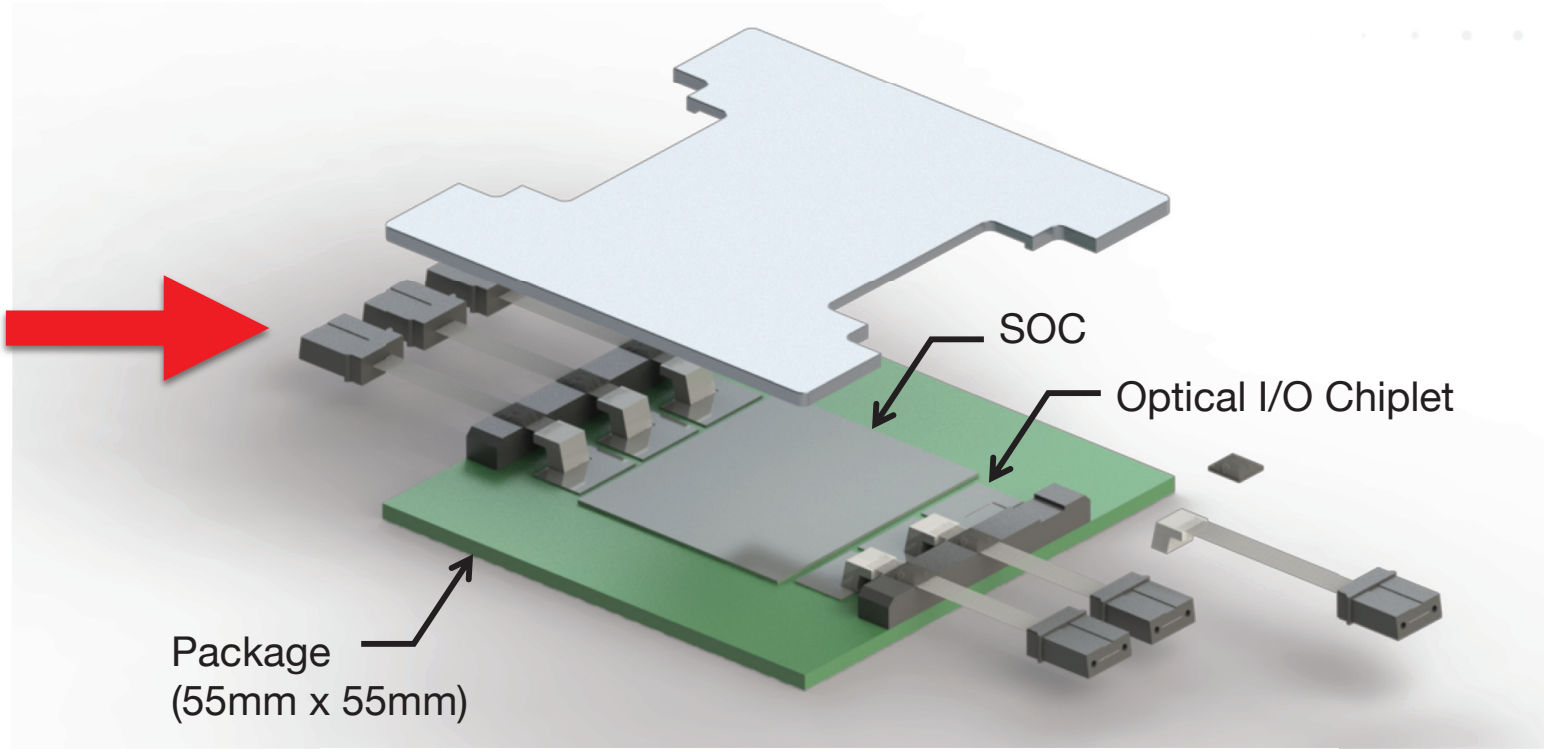
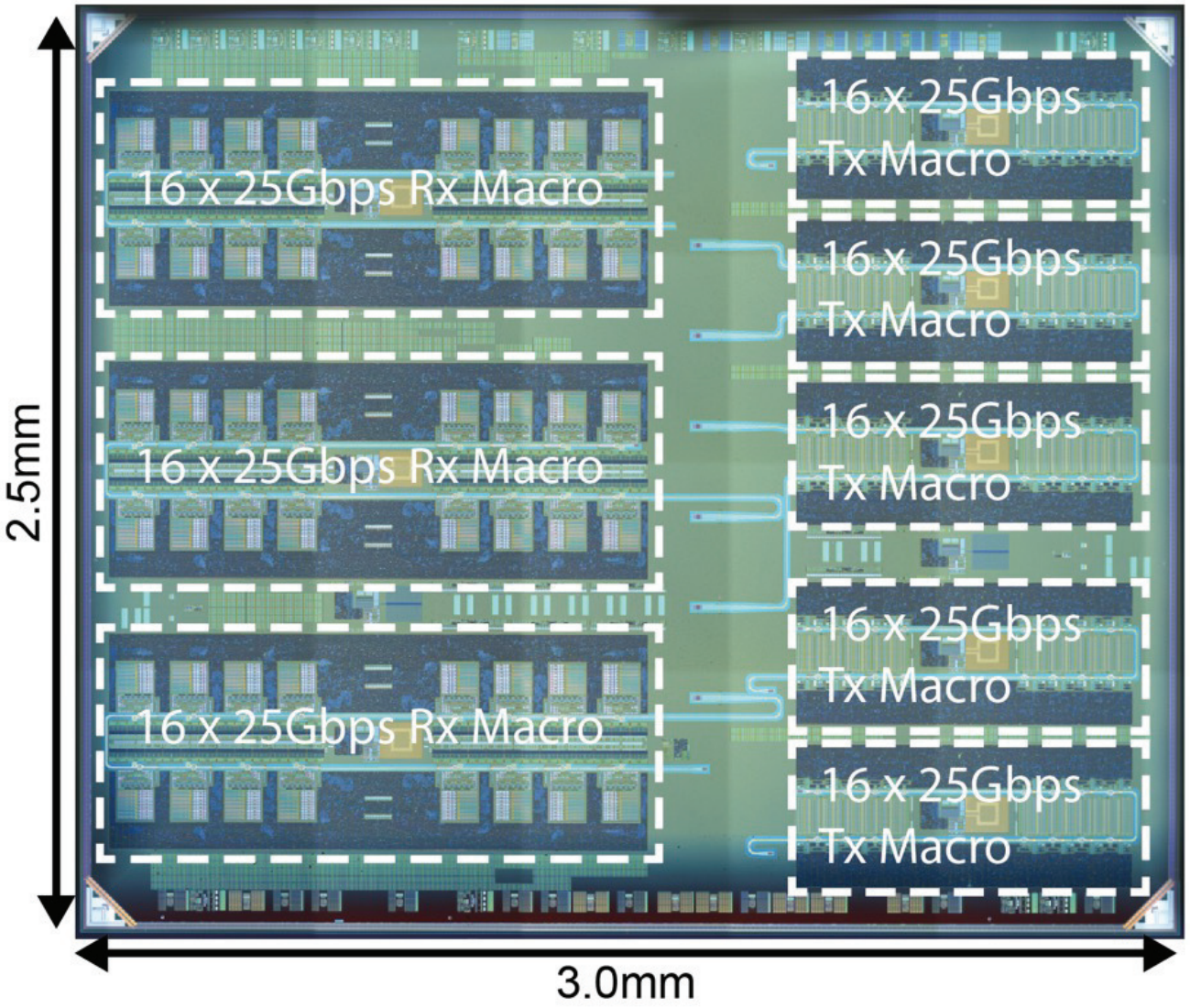


Co-packaged optical I/O
for 10 – 100+ Tbps I/O



TeraPHY: A Chiplet for Optical I/O



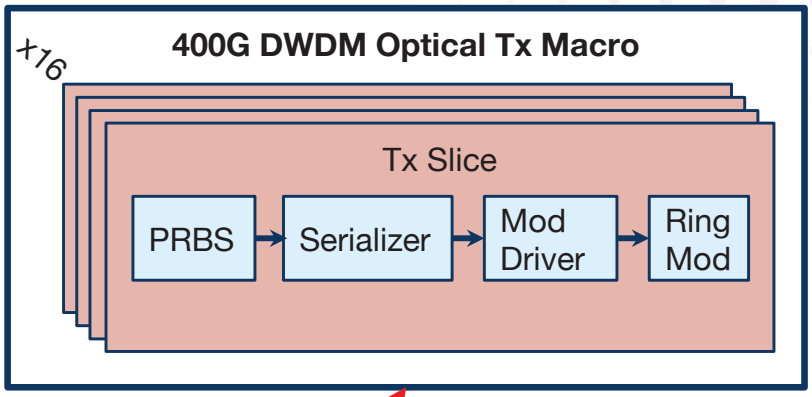
- Monolithic circuits and photonics in 45nm SOI
- Circuits contain all analog, digital, PLLs, clocking needed
- Process transistor performance fast enough to achieve 112Gbps serial line rates
- External laser

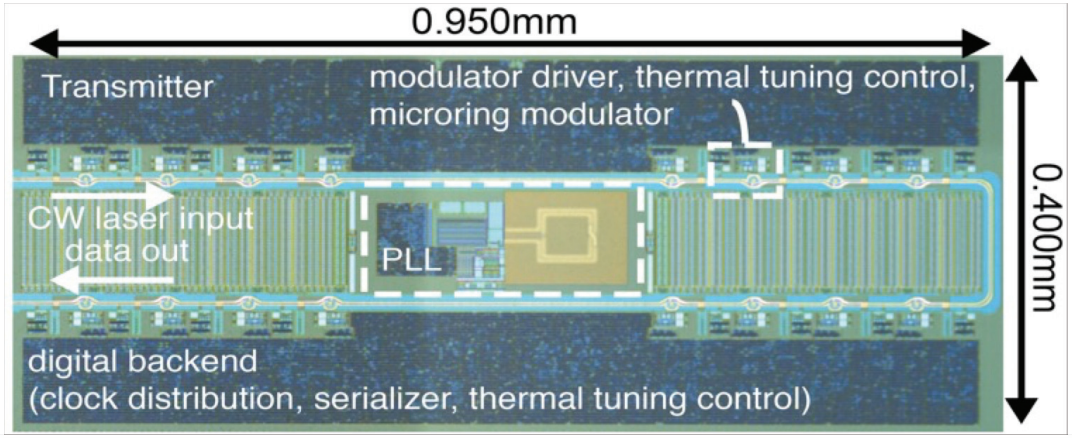
Constraints of Co-packaged Optics

- Bandwidth density
  - Need >100Gbps/mm2 of optical bandwidth density
- Power efficiency
  - <2pJ/bit dissipated in the package (100W at 50Tb/s)
- Thermal environment
  - Up to 400W dissipated and 115ºC in the package
- Co-packaging complexity
  - Need to simplify package!

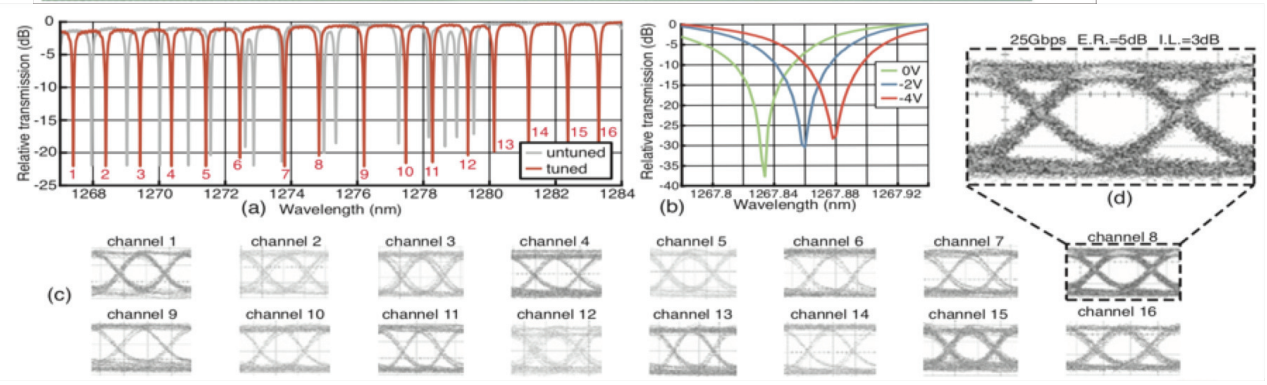
TeraPHY: Optics Power Efficiency

- Power efficiency
  - <2pJ/bit dissipated in the package
  - Microring-based transceivers are energy efficient
  - Multiple demonstrations showing sub-pJ/bit transmit and receive, including thermal tuning
  - [Moazeni 2017, Mehta 2016, Stojanovic 2018]





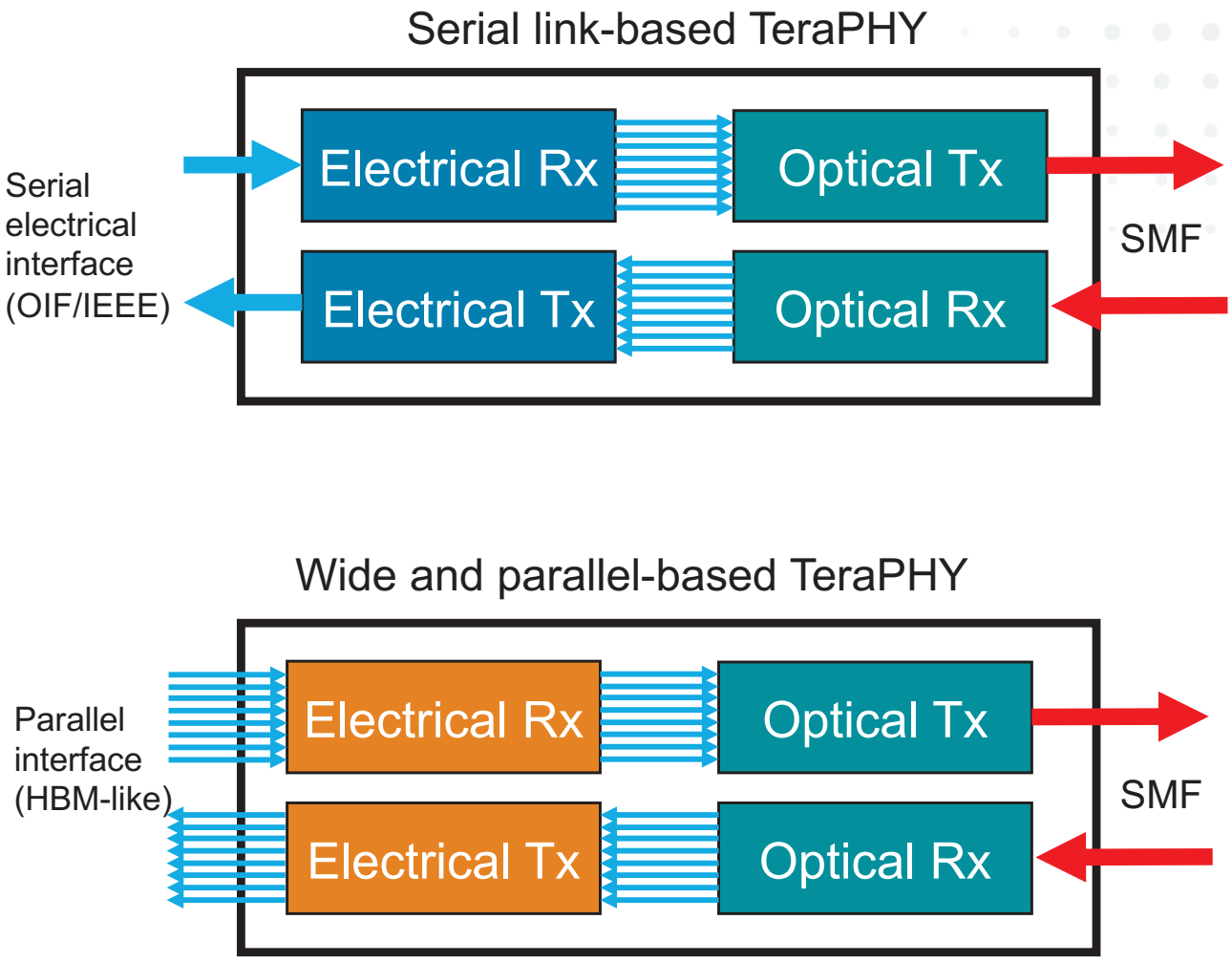
- 16 channels
- >1 Tbps/mm²
- 0.8 pJ/bit



Tx Power Consumption	Power [mW]	Energy [pJ/bit]
LC-PLL	30.5	0.08
Clock Distribution	86.2	0.21
Tuning Controllers	20.0	0.05
Ring Heater Drivers	20.5	0.05
$4V_{pp}$ Driver	6.8 (per slice)	0.27
Serializer	4.0 (per slice)	0.16
Total:	330	**0.83**

TeraPHY: Wide Parallel Electrical I/O

- Integration of photonics in CMOS enables digital interface to photonic links
  - On-chip bus between electronics and optics is a parallel digital bus
- Supports:
  - fast and serial (OIF/IEEE) electrical interfaces
  - wide and parallel (HBM-like) interfaces to drive down electrical I/O to <1pJ/bit



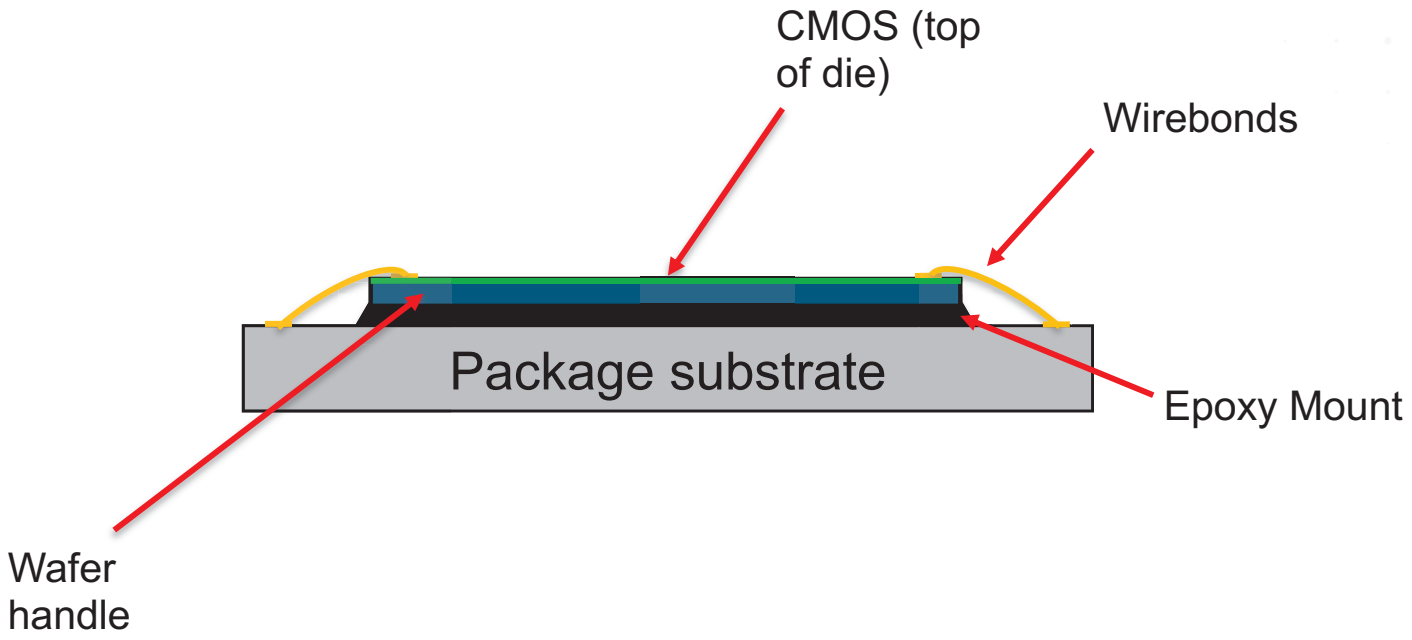
Constraints of Co-packaged Optics

- Bandwidth density
  - Need >100Gbps/mm2 of optical bandwidth density
- Power efficiency
  - <2pJ/bit dissipated in the package (100W at 50Tb/s)
- Thermal environment
  - Up to 400W dissipated in the package, this is hot
- Co-packaging complexity
  - Need to simplify package!

TeraPHY: Packaging Simplicity

- Requirements:
  - Minimize number of components
  - Electrical packaging must be accomplished using existing tools
  - Fiber attach must be scalable to high volume
  - Must be compliant with co-packaging processes

Problems with Fiber Attach: Wirebonded Chips



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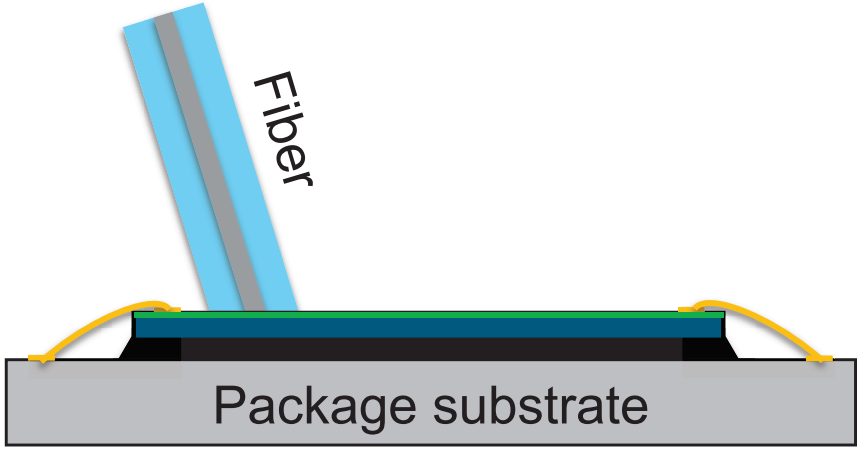
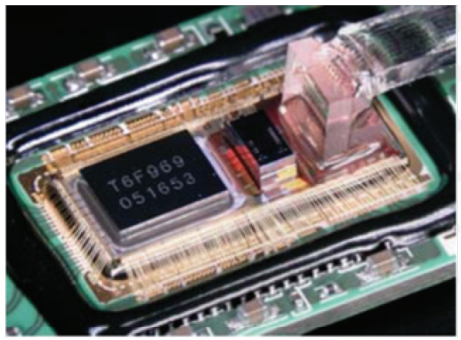
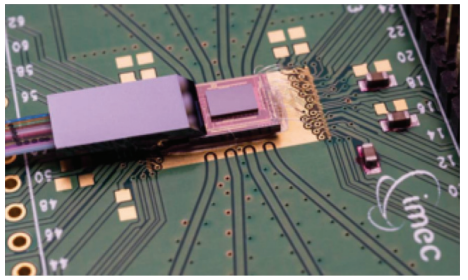




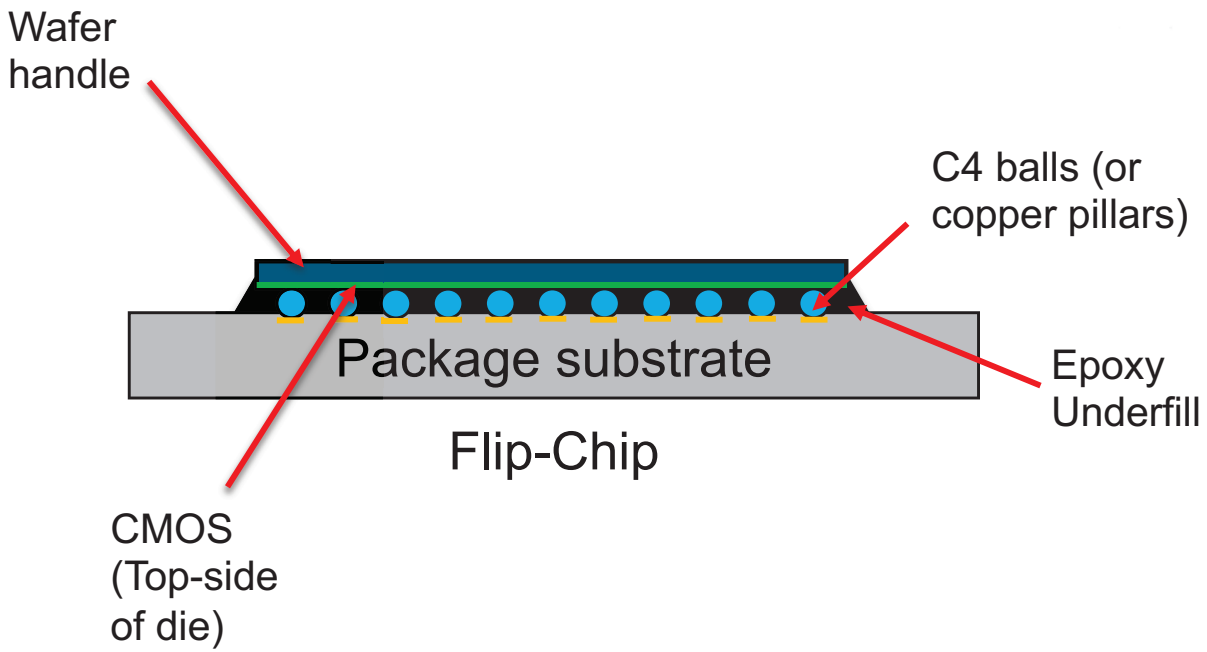
[Luxtera]



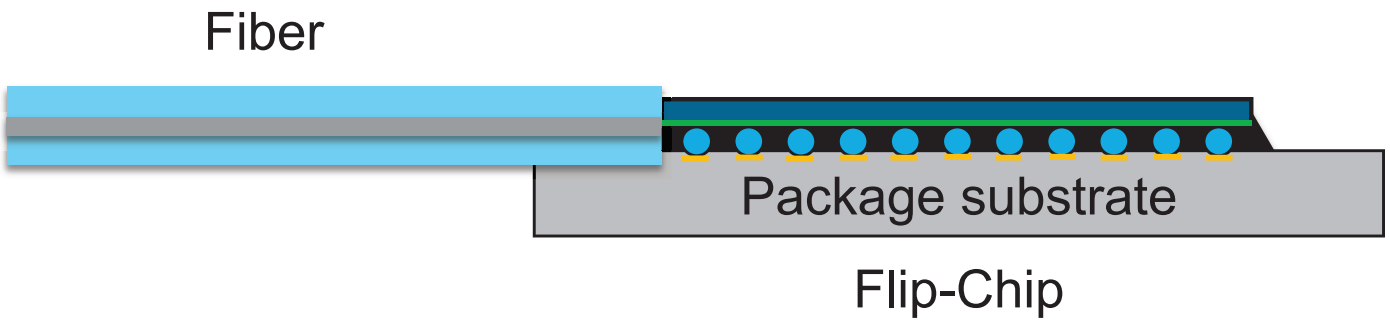
[Imec]

- Currently the SiPh dominant packaging method
- You will need thousands of wirebonds per co-packaged chiplet
- Works for standalone transceivers, not scalable for co-packaged form factor! Need to be flip-chip compatible!

Problems with Fiber Attach: Flip-Chip

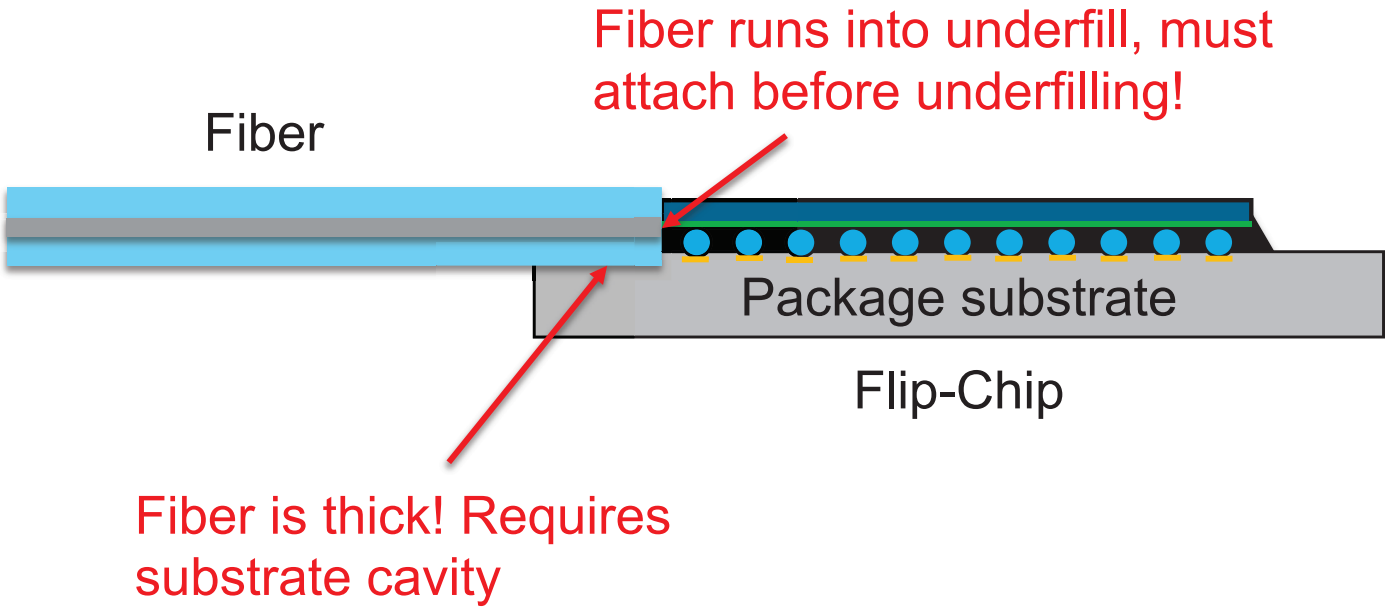


Problems with Fiber Attach: Flip-Chip + Edge



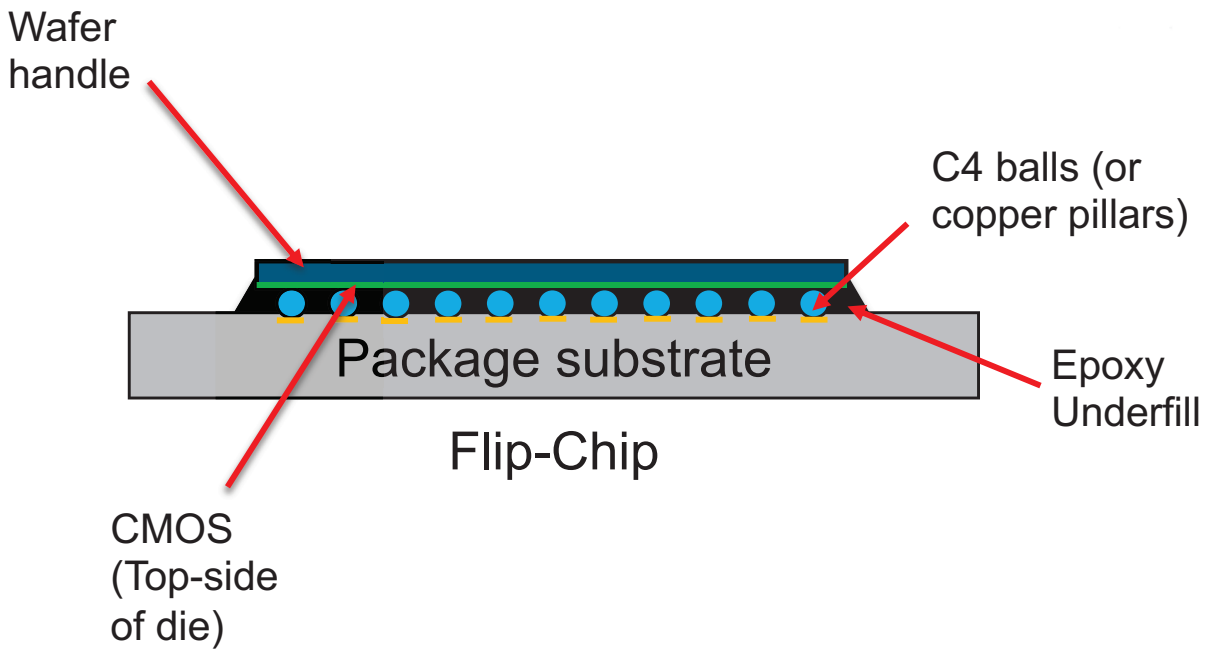
Flip-Chip

Problems with Fiber Attach: Flip-Chip + Edge

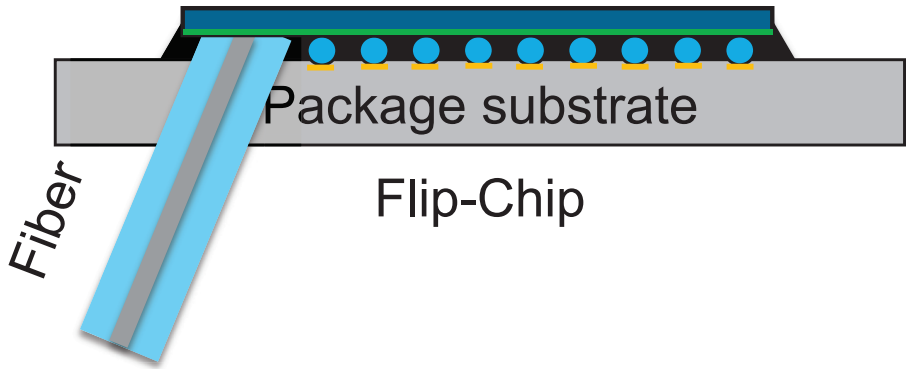


- Edge coupling breaks many parts of the flip-chip flow
  - Package needs cavity
  - Must do the attach before flip-chip assembly

Problems with Fiber Attach: Flip-Chip

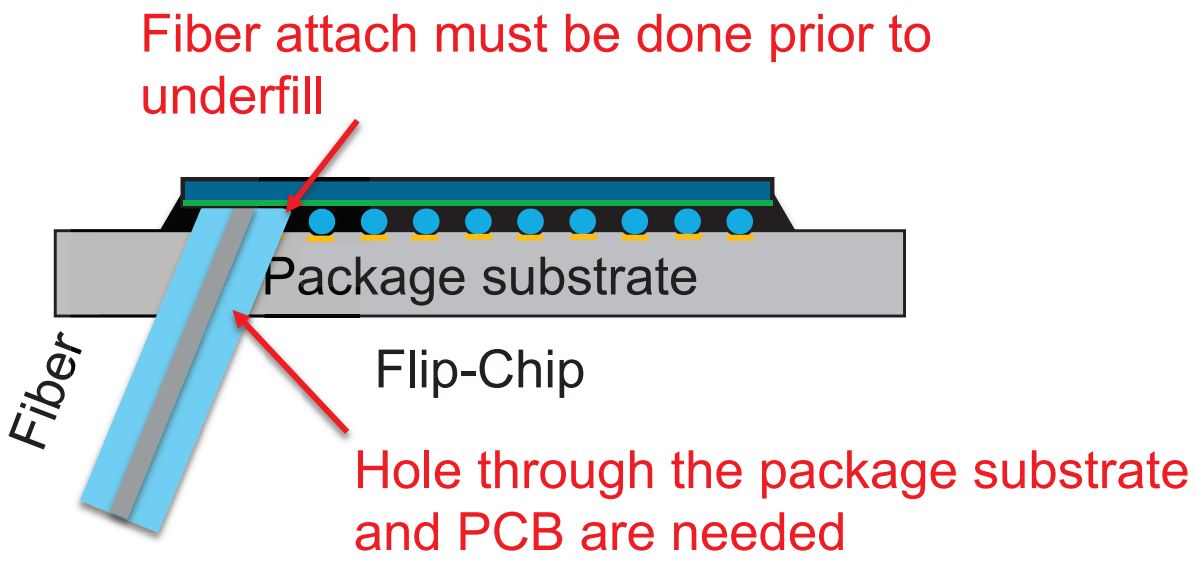


Problems with Fiber Attach: Flip-Chip + Vertical



- Vertical coupling breaks even more parts of the flip-chip assembly flow

Problems with Fiber Attach: Flip-Chip + Vertical

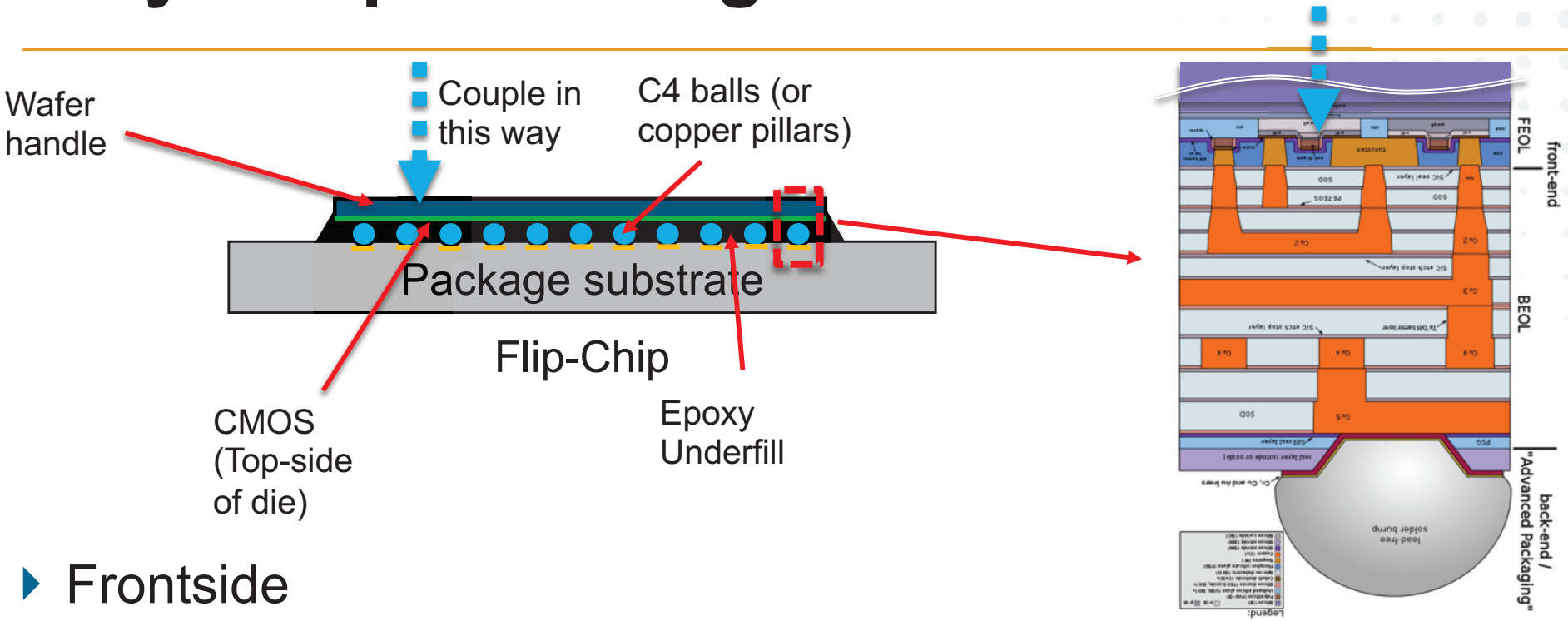


- Vertical coupling breaks even more parts of the flip-chip assembly flow

So what do we do?

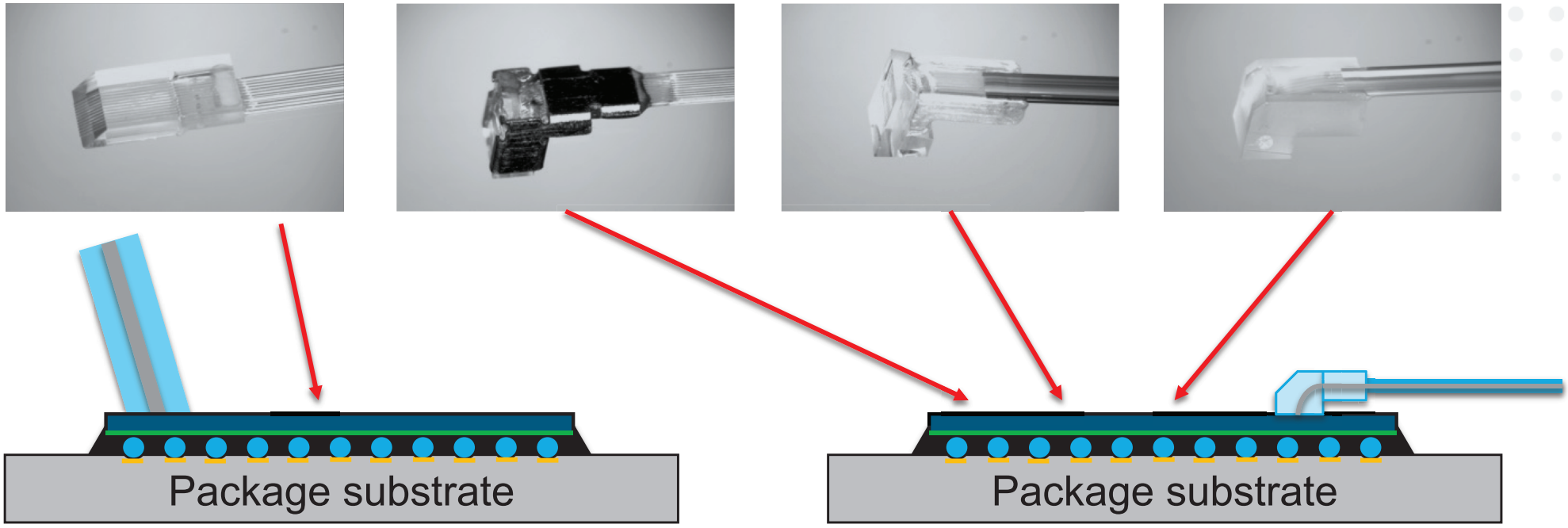
- Wirebond assembly does not scale to MCMs
- Neither contemporary edge nor vertical attach works for flip-chip assembly flow
- TeraPHY Solution: Backside attach!

Why Couple Through Backside?



- Frontside
  - Wirebond / flip-chip package / assembly flow is not compatible
  - ILD and “metal fill” creates discontinuities in propagation path
- Backside
  - No obstructions to the chip backside
    - Remember: silicon is transparent at 1100+ nm wavelengths
  - Uniform & transparent structure (not dependent on CMOS metal stack)

Fiber Arrays – Standard Form Factors

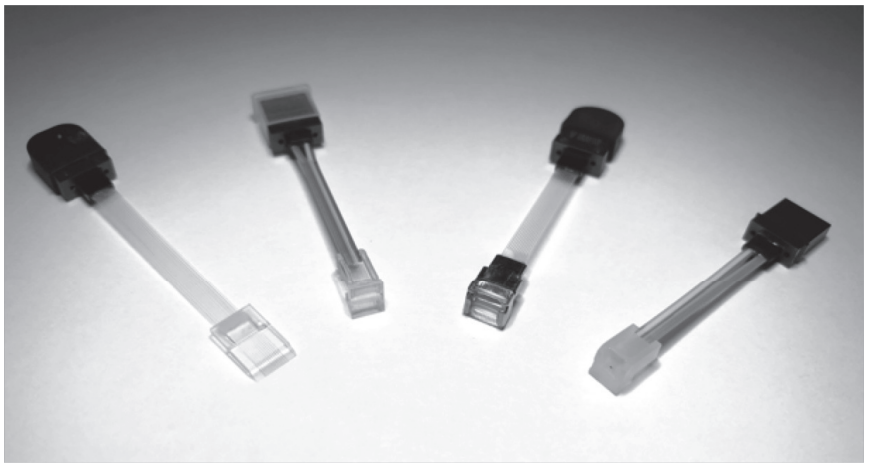


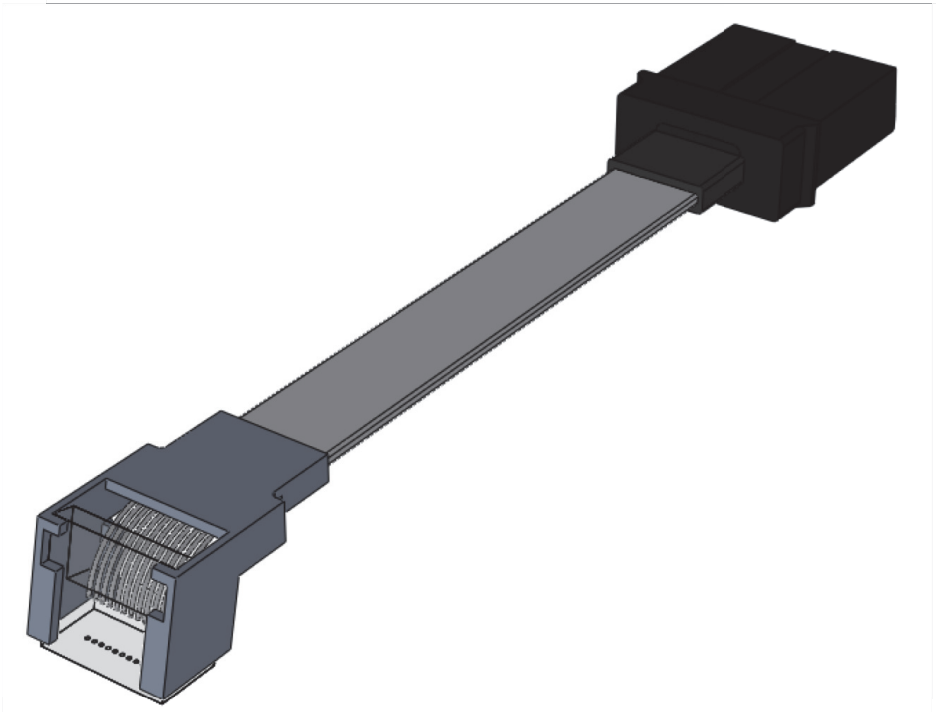
Vertical direct attach

Bent fiber array attach

- Standard form factors work well with backside attach method
  - Leverage existing ecosystem
- However, still several mechanical downsides!

“Low Profile” Fiber Arrays

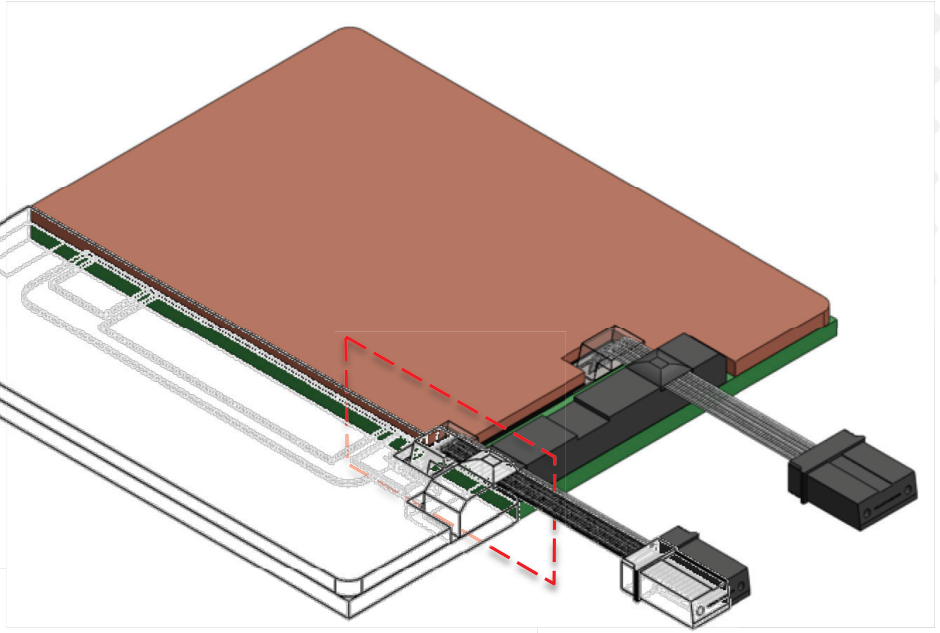


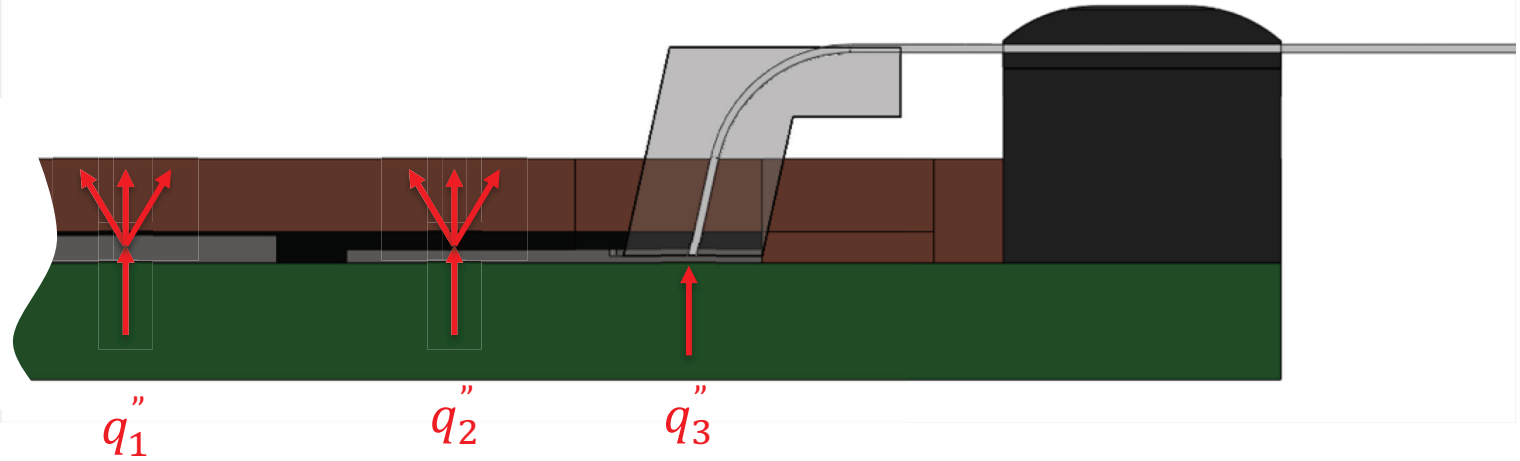


- Up to 12-f available
- 3.75 – 4.2 mm profile
  - Limit: ~R_{min} ≅ 3 mm
  - Many vendors with similar profile
- “Low profile” is still too big and too tall

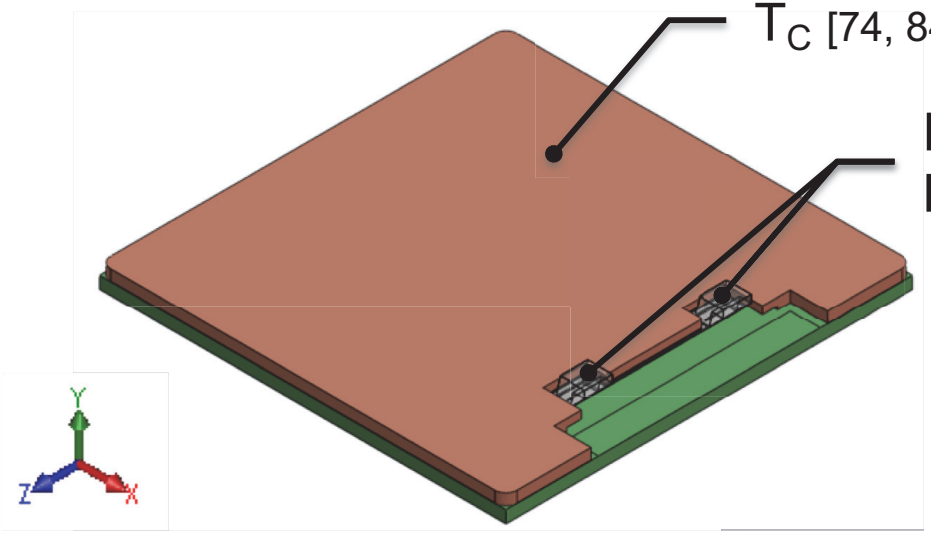
Fiber Array Thermal Resistance

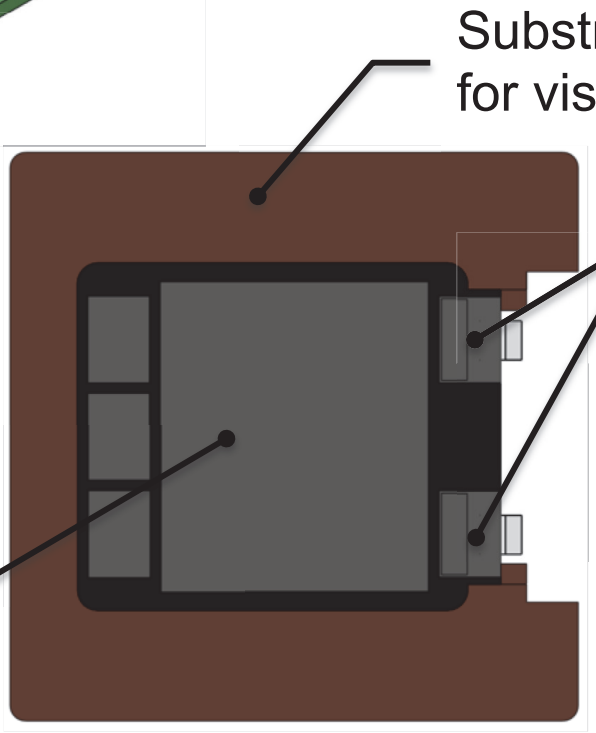
- Fiber array impacts thermal resistance
- Heat sink needs cutout to support fiber array!
- Minimize dissipation under fiber array
- Height scaling limit
  - Bend radius limits height





Boundary Conditions

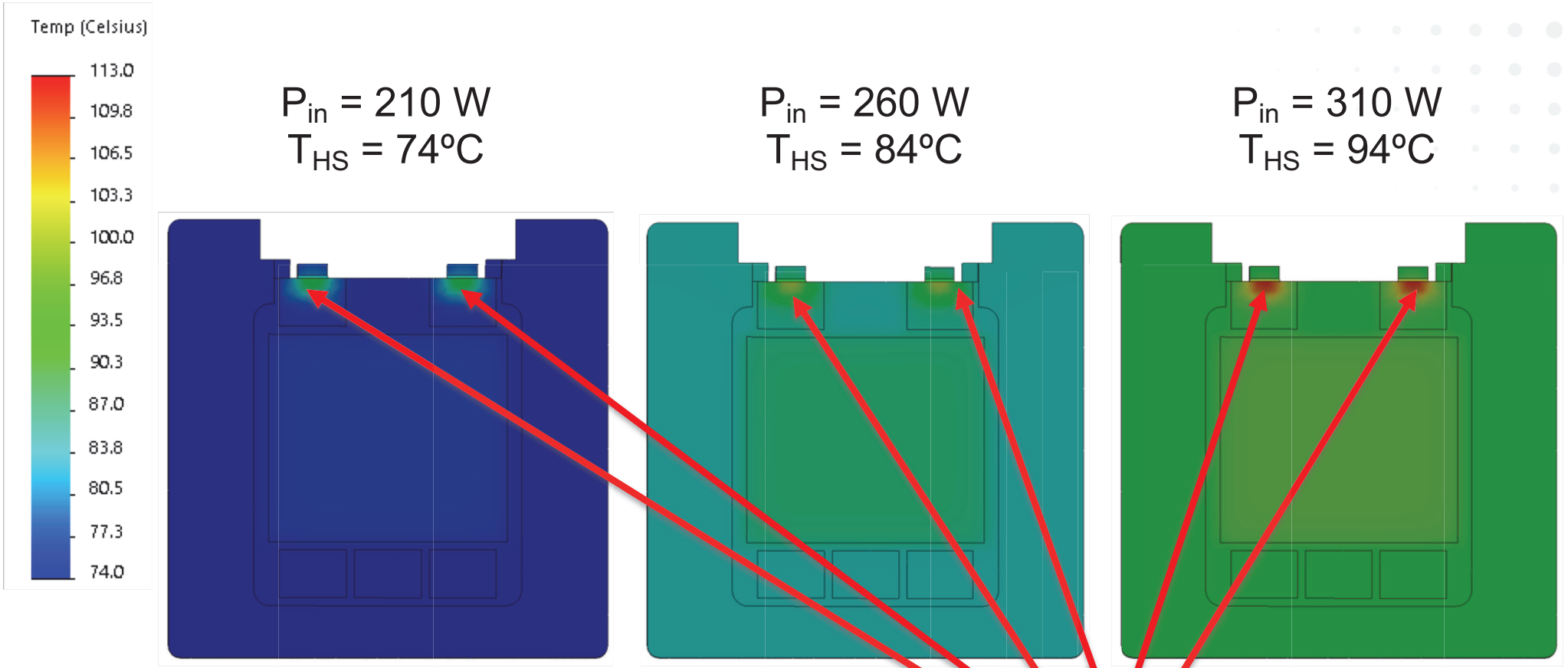




$\rho_{SOC} \cong 0.26$ W/mm^2

$\rho_{TeraPHY} \cong 0.1$ W/mm^2

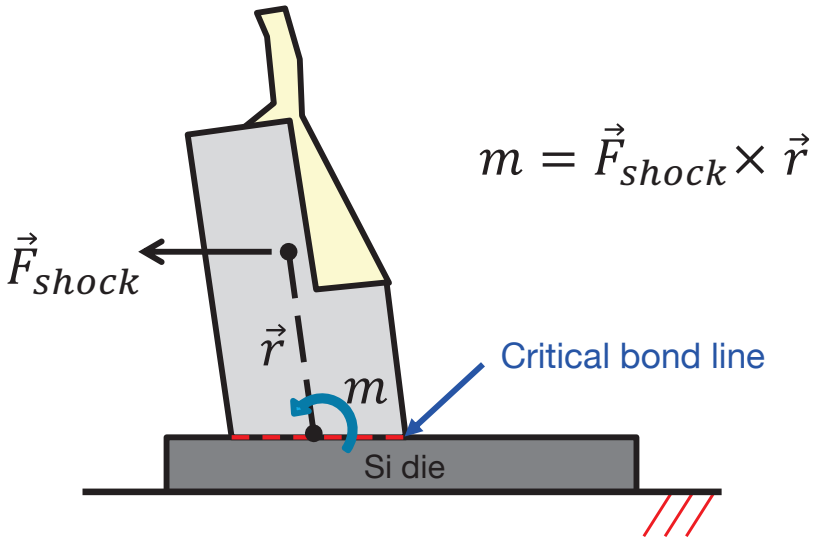
Thermal Implications of “low profile” connector



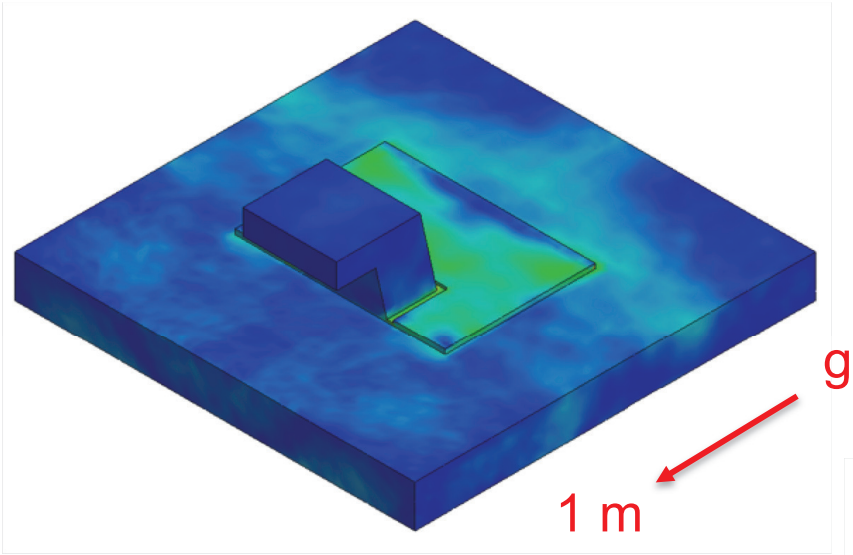
- Analysis assumes uniform SOC power
- Analysis assumes uniform TeraPHY

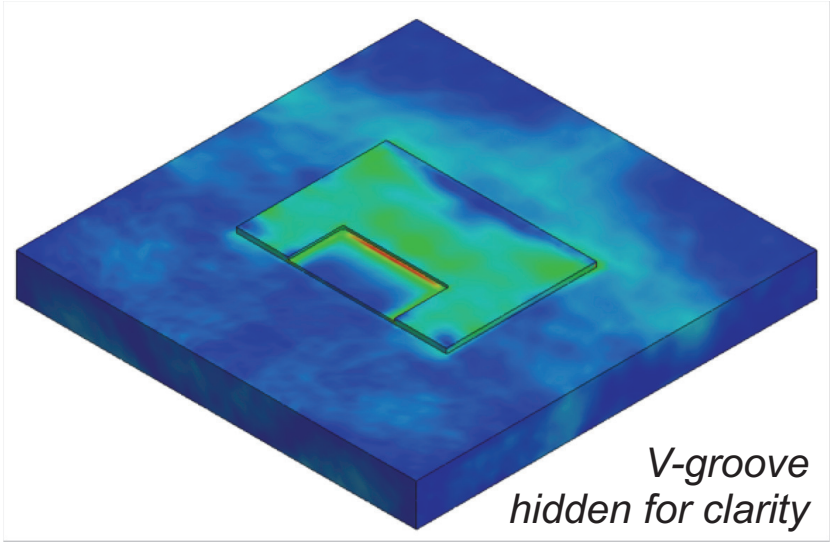
High heat concentration near fiber connector

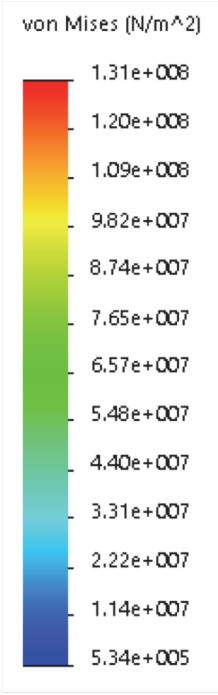
Mechanical Implications: Drop Testing



$$m = \vec{F}_{shock} \times \vec{r}$$

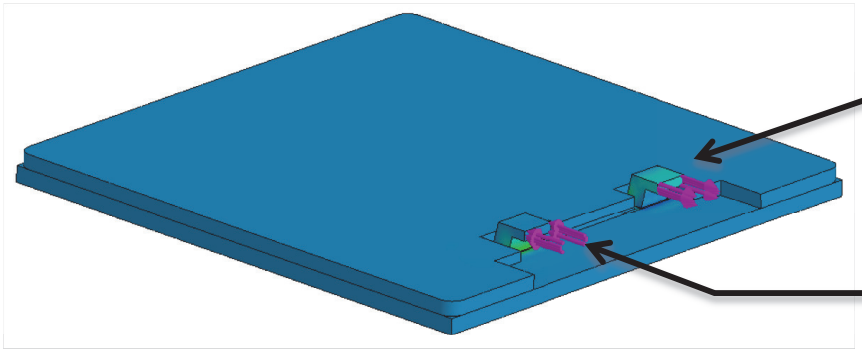




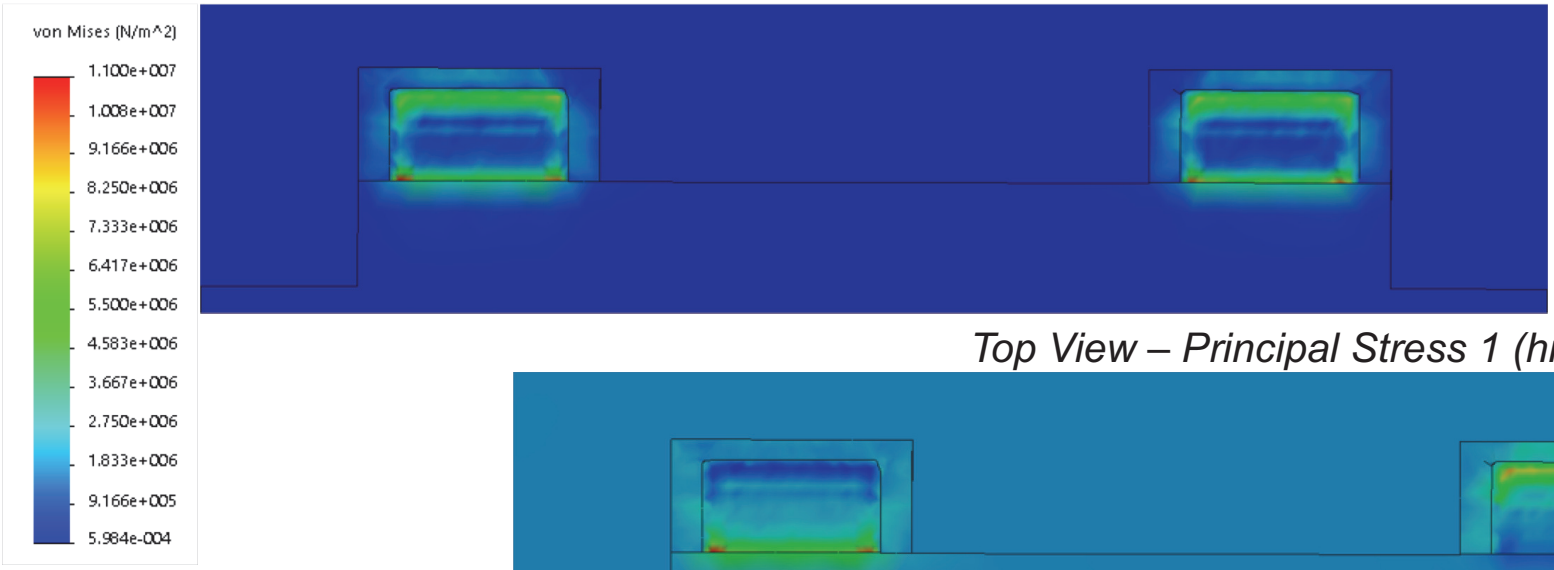


- Drop testing simulation
- Sub-model focusing on fiber array interaction with die
- $\sigma_{\text{von Mises}}$ ~ 131 MPa

Mechanical Implications: Static Fiber Pull

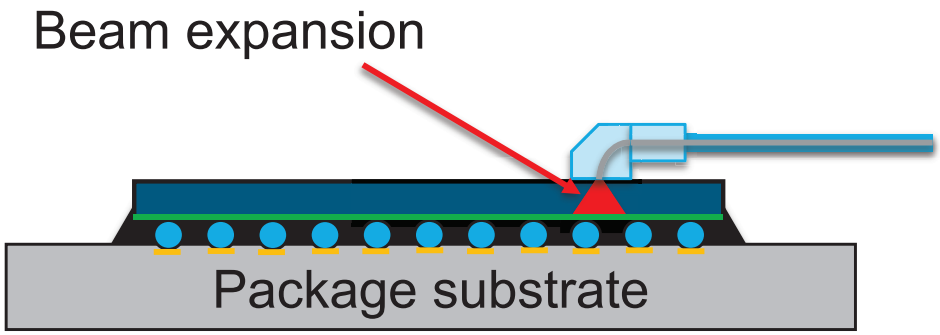


Top View – von Mises (hidden fiber array)



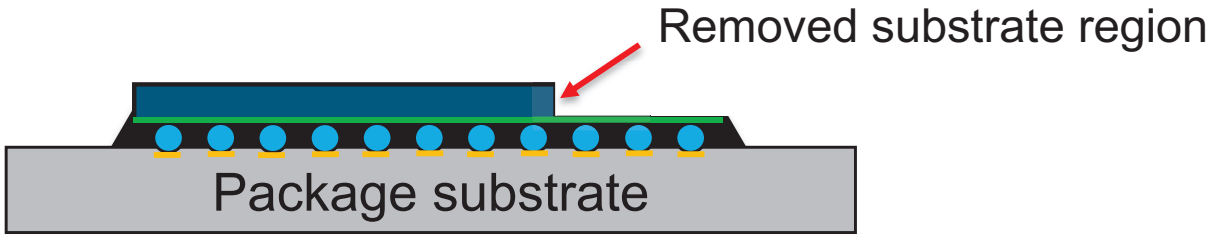
Top View – Principal Stress 1 (hidden fiber array)

Fiber Array Shortfalls: Working Distance



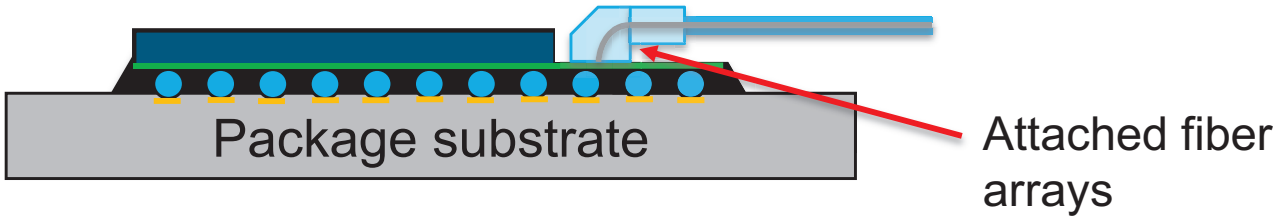
- Problem: beam expands as it travels height of the substrate
  - 50um distance will add an extra 1dB to coupling losses

Fiber Array Shortfalls: Working Distance



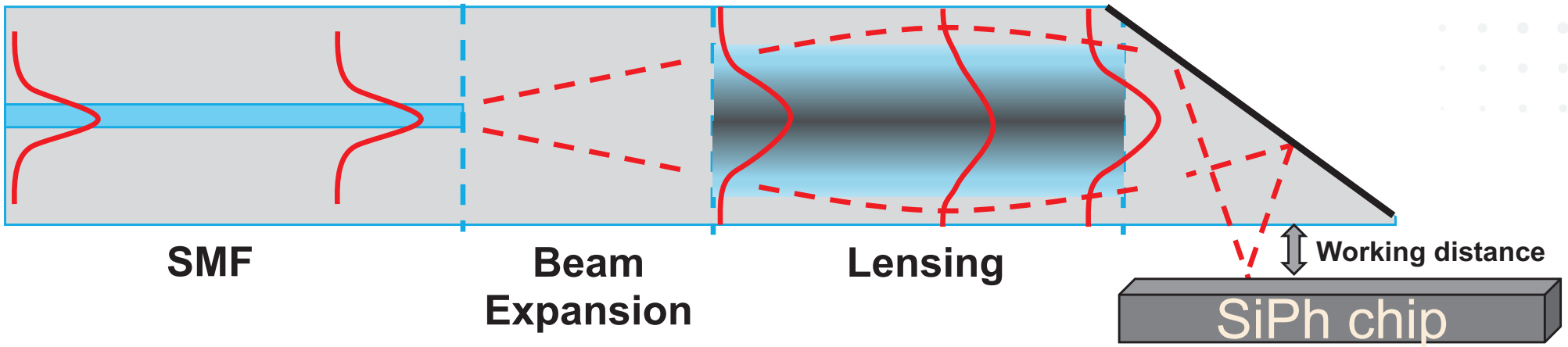
- Current solution: thin/remove substrate over attach points
  - Fiber array attaches directly to the CMOS, working distance minimized
  - Side benefit: Etching pattern can used substrate edge as passive guide for passive alignment

Fiber Array Shortfalls: Working Distance



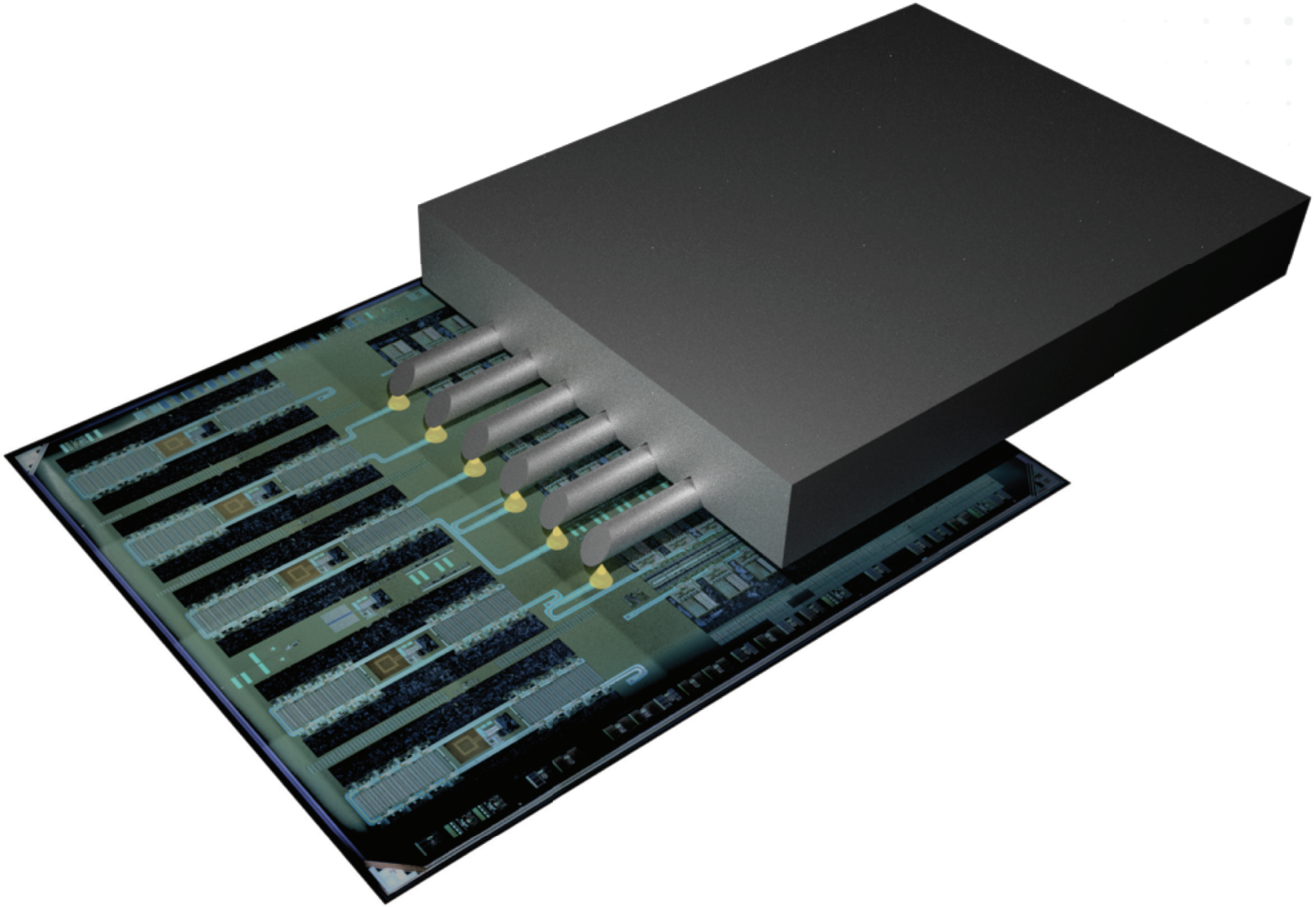
- Current solution: thin/remove substrate over attach points
  - Fiber array attaches directly to the CMOS, working distance minimized
  - Side benefit: Etching pattern can used substrate edge as passive guide for passive alignment

TeraPHY: micro GRIN for Fiber Attach

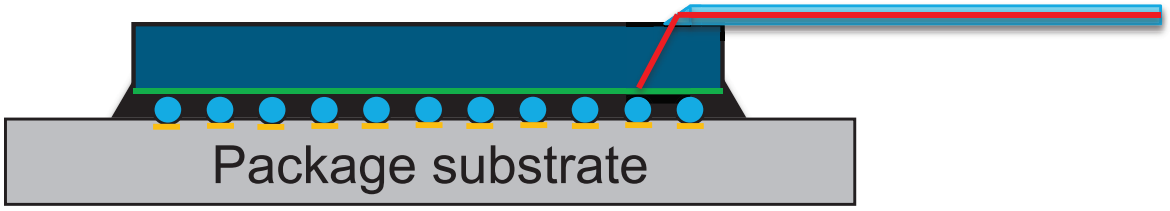


- micro GRIN elegantly combines beam-turning and lensing
  - Design and control beam size, and
  - Working distance to chip
  - Ultimate in low profile fiber coupling

micro GRIN for Fiber Attach

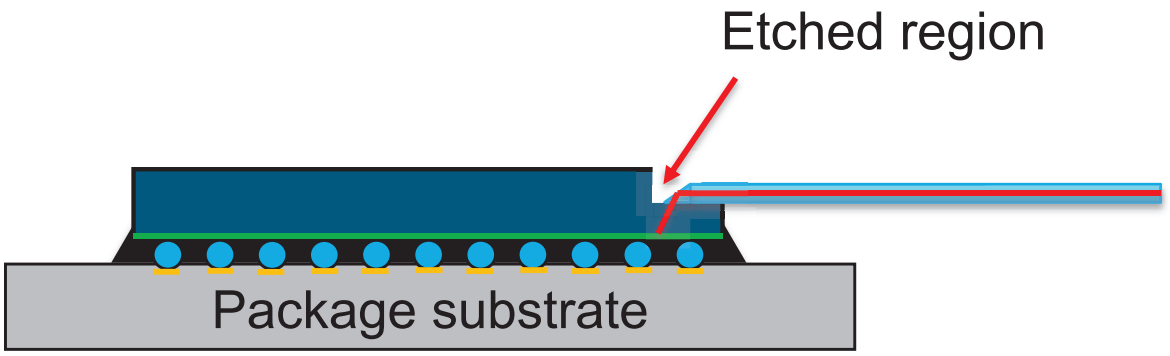


MicroGRIN Attach



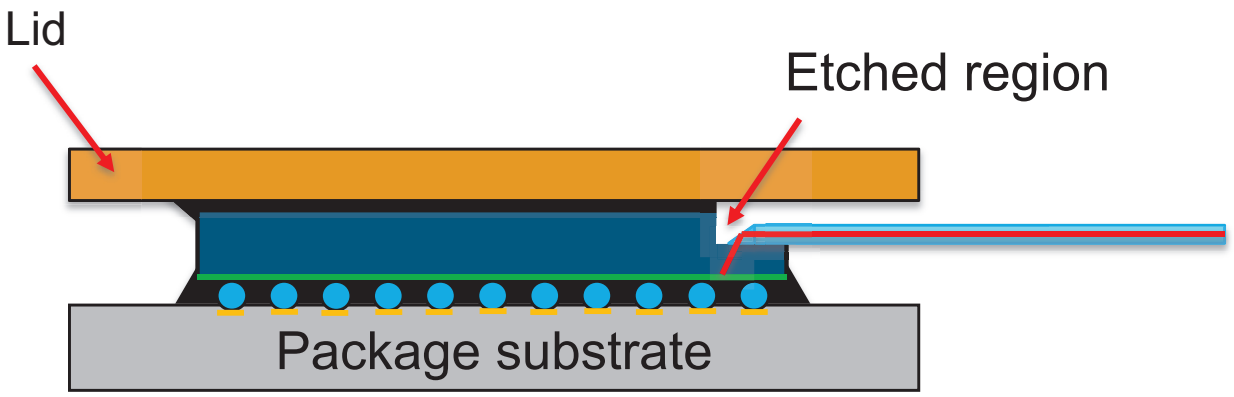
- Lensing structure of MicroGRIN solves the beam expansion through substrate issue

MicroGRIN Attach



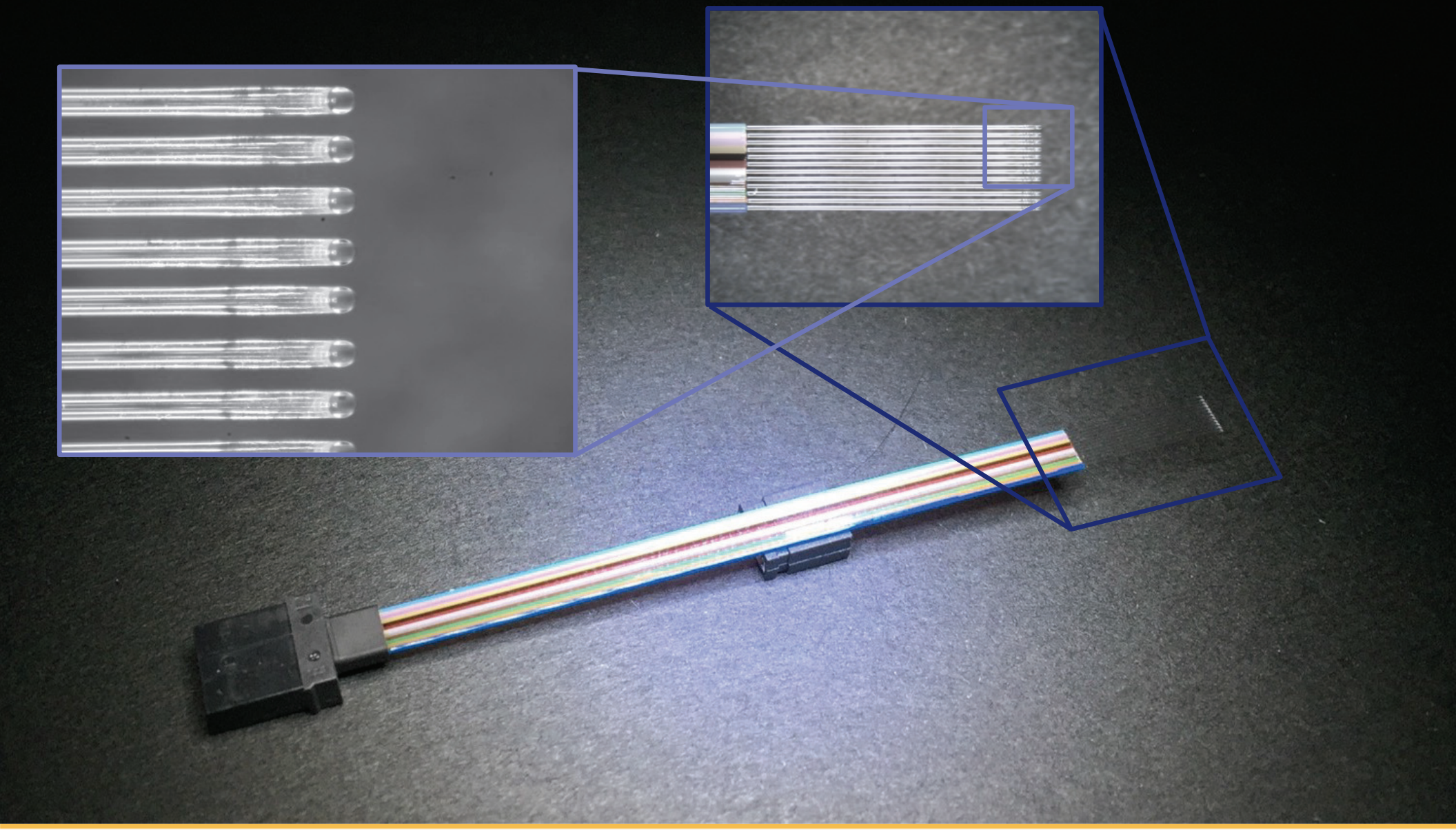
- Use etching as additional step
  - A step towards complete passive alignment
  - Die thickness in etched regions can be large enough to maintain structural integrity

MicroGRIN Attach

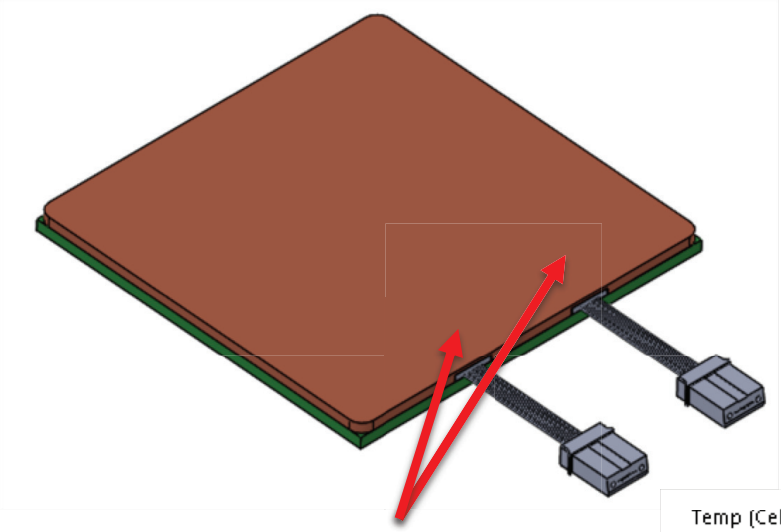


- Use etching as additional step
  - A step towards complete passive alignment
  - Die thickness in etched regions can be large enough to maintain structural integrity
  - micro GRIN can hide within the etched region, not intrude on lid design

Fabricated micro GRIN



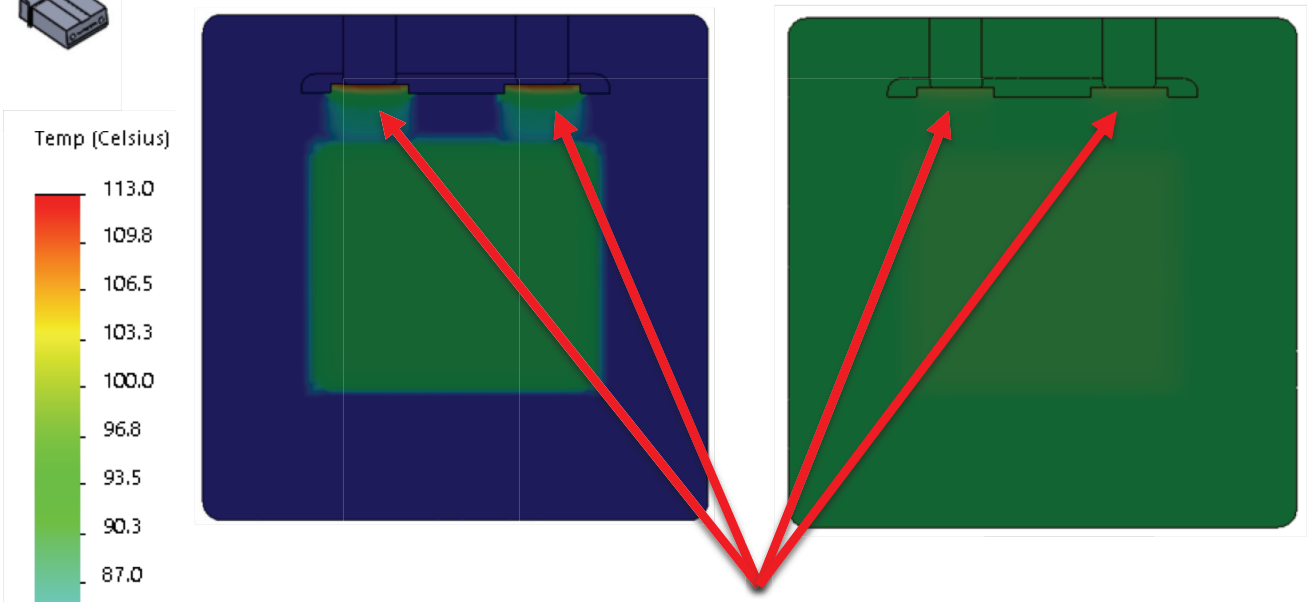
Thermals are much better with micro GRIN!



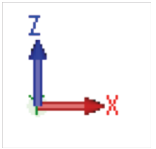
micro GRIN under lid (protected)

P_{in} = 210 W
T_{HS} = 74ºC

P_{in} = 310 W
T_{HS} = 94ºC

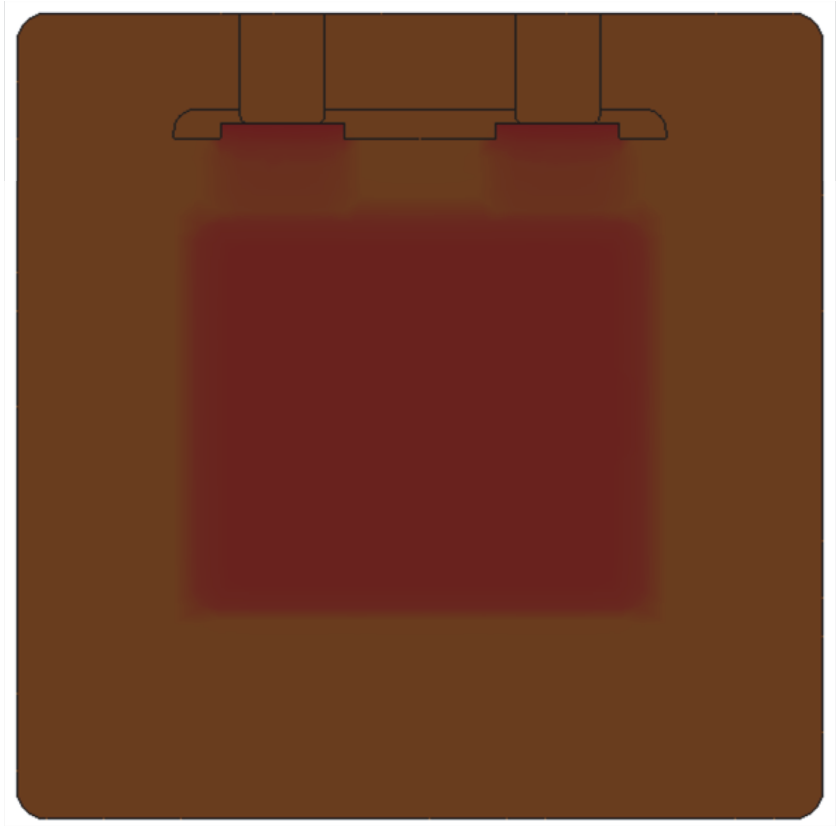


Thermals under microGRIN are much better



Managing 380W with Same Heat Sink

P_{in} = 380 W
T_{HS} = 108ºC

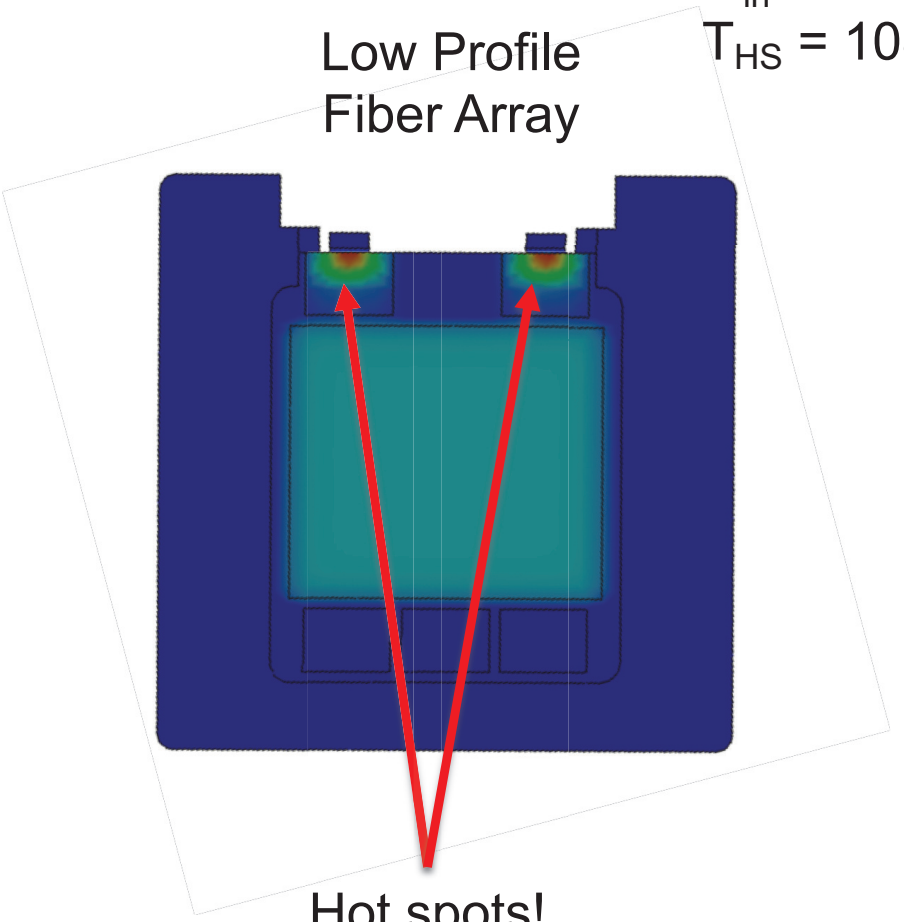


Customers requesting 115ºC!

Fiber Array vs. micro GRIN Thermals

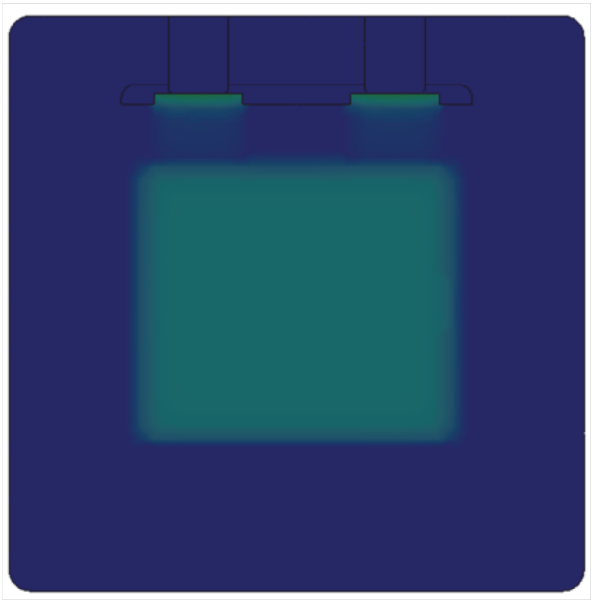
P_{in} = 380 W
T_{HS} = 108ºC

Low Profile
Fiber Array

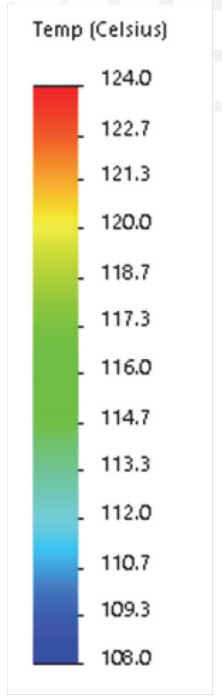


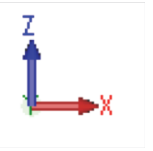
Hot spots!

micro GRIN



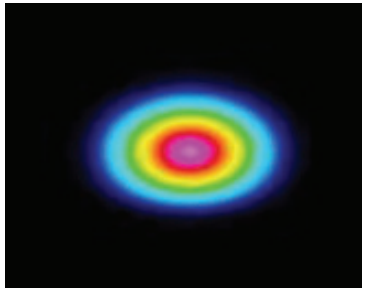
No Hot Spots



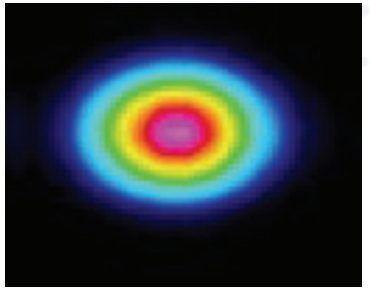


micro GRIN Status

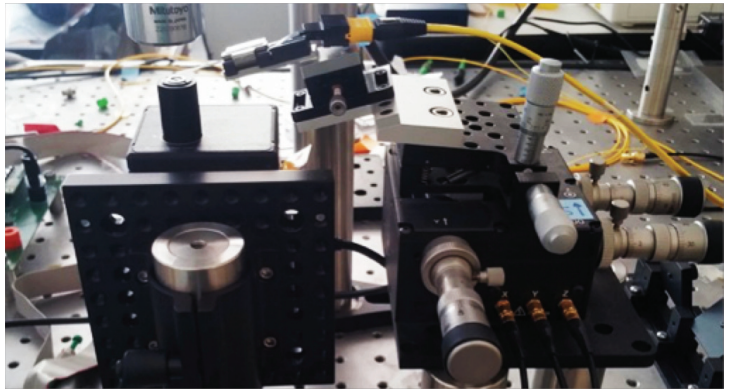
- micro GRIN to die coupling
  - < 3dB insertion loss
- Automated beam profiling
  - Integrated COTS instrumentation
- Manufacturability
  - Empirically resolved beam profile variation
  - Resolved error in angle bias
  - Developed first generation coating



Example Beam Profile(s)



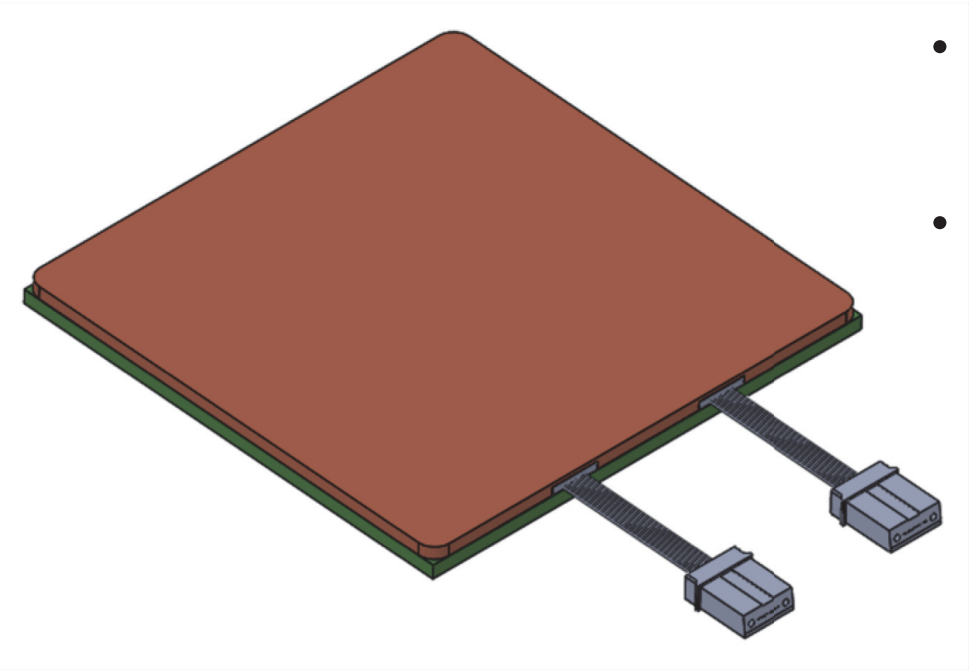
Beam Profile Setup



T2M Activities

- Planned Intellectual Property
  - "Fiber Attach Enabled Wafer Level Fanout"
  - "Wafer Level Handle and Hard Mask Processing"
- Planned Publications
  - OFC – "TeraPHY: A high-density electronic-photonic chiplet for co-packaged optical I/O"
  - ECTC – "Heterogenous Integration of Silicon Photonics"
- Commercialization
  - Demonstration 2H'19 with partner

ENLITENED Achievements



- Fiber Attach
  - Low Profile Fiber Arrays
  - micro GRIN
- Package Design
  - Thermal Management
  - Material Selection
- Assembly Process Flow
  - MCM compatibility
  - Backside pattern & etch
- Chip Design
  - Improved design flow
  - Simulation of couplers with micro GRIN

Conclusion

- Electrical I/O scaling is at a scaling end and optical I/O is the only viable alternative
- Current technologies used in predominantly pluggable optics are far from achieving specs needed for a co-packaged optical I/O technology
  - Density, power, packaging are all falling far short of requirements
- The TeraPHY chiplet-based architecture fulfills many of the requirements for co-packaged optical I/O
- Backside fiber attach using microGRIN achieves the packaging simplicity to co-package the TeraPHY with high-performance SoCs
- Next step: Demonstrate TeraPHY with 3rd party SoC
  - Demonstration platform already underway with partner

Thank you!